

GIGABYTE™

R262-ZA1

R262-ZA2

AMD EPYC™ 7002 UP Server System - 2U 14-Bay

User Manual

Rev. 1.0

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Documentation Classifications

In order to assist in the use of this product, GIGABYTE provides the following types of documentation:

- User Manual: detailed information & steps about the installation, configuration and use of this product (e.g. motherboard, server barebones), covering hardware and BIOS.
- User Guide: detailed information about the installation & use of an add-on hardware or software component (e.g. BMC firmware, rail-kit) compatible with this product.
- Quick Installation Guide: a short guide with visual diagrams that you can reference easily for installation purposes of this product (e.g. motherboard, server barebones).

Please see the support section of the online product page to check the current availability of these documents.

For More Information

For related product specifications, the latest firmware and software, and other information please visit our website at <http://www.gigabyte.com>




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For any general sales or marketing enquiries, you may also message GIGABYTE server directly by email: server.grp@gigabyte.com

Conventions

The following conventions are used in this user's guide:

	<p>NOTE!</p> <p>Gives bits and pieces of additional information related to the current topic.</p>
	<p>CAUTION!</p> <p>Gives precautionary measures to avoid possible hardware or software problems.</p>
	<p>WARNING!</p> <p>Alerts you to any damage that might result from doing or not doing specific actions.</p>

Server Warnings and Cautions

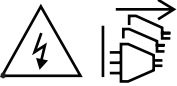
Before installing a server, be sure that you understand the following warnings and cautions.



WARNING!

To reduce the risk of electric shock or damage to the equipment:

- Do not disable the power cord grounding plug. The grounding plug is an important safety feature.
- Plug the power cord into a grounded (earthed) electrical outlet that is easily accessible at all times.
- Unplug all the power cords from the power supplies to disconnect power to the equipment.



- Unplug the power cord from the power supply to disconnect power to the equipment.
- Do not route the power cord where it can be walked on or pinched by items placed against it. Pay particular attention to the plug, electrical outlet, and the point where the cord extends from the server.



WARNING!

To reduce the risk of personal injury from hot surfaces, allow the drives and the internal system components to cool before touching them.



WARNING!

This server is equipped with high speed fans. Keep away from hazardous moving fan blades during servicing.



WARNING!

This equipment is intended to be used in Restrict Access Location. The access can only be gained by Skilled person.

Only authorized by well trained professional person can access the restrict access location.



CAUTION!

- Do not operate the server for long periods with the access panel open or removed. Operating the server in this manner results in improper airflow and improper cooling that can lead to thermal damage.
- Danger of explosion if battery is incorrectly replaced.
- Replace only with the same or equivalent type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

Electrostatic Discharge (ESD)



CAUTION!

ESD CAN DAMAGE DRIVES, BOARDS, AND OTHER PARTS. WE RECOMMEND THAT YOU PERFORM ALL PROCEDURES AT AN ESD WORKSTATION. IF ONE IS NOT AVAILABLE, PROVIDE SOME ESD PROTECTION BY WEARING AN ANTI-STATIC WRIST STRAP ATTACHED TO CHASSIS GROUND -- ANY UNPAINTED METAL SURFACE -- ON YOUR SERVER WHEN HANDLING PARTS.

Always handle boards carefully. They can be extremely sensitive to ESD. Hold boards only by their edges without any component and pin touching. After removing a board from its protective wrapper or from the system, place the board component side up on a grounded, static free surface. Use a conductive foam pad if available but not the board wrapper. Do not slide board over any surface.

System power on/off: To remove power from system, you must remove the system from rack. Make sure the system is removed from the rack before opening the chassis, adding, or removing any non hot-plug components.

Hazardous conditions, devices and cables: Hazardous electrical conditions may be present on power, telephone, and communication cables. Turn off the system and disconnect the cables attached to the system before servicing it. Otherwise, personal injury or equipment damage can result.

Electrostatic discharge (ESD) and ESD protection: ESD can damage drives, boards, and other parts. We recommend that you perform all procedures in this chapter only at an ESD workstation. If one is not available, provide some ESD protection by wearing an antistatic wrist strap attached to chassis ground (any unpainted metal surface on the server) when handling parts.

ESD and handling boards: Always handle boards carefully. They can be extremely sensitive to electrostatic discharge (ESD). Hold boards only by their edges. After removing a board from its protective wrapper or from the system, place the board component side up on a grounded, static free surface. Use a conductive foam pad if available but not the board wrapper. Do not slide board over any surface.

Installing or removing jumpers: A jumper is a small plastic encased conductor that slips over two jumper pins. Some jumpers have a small tab on top that can be gripped with fingertips or with a pair of fine needle nosed pliers. If the jumpers do not have such a tab, take care when using needle nosed pliers to remove or install a jumper; grip the narrow sides of the jumper with the pliers, never the wide sides. Gripping the wide sides can damage the contacts inside the jumper, causing intermittent problems with the function controlled by that jumper. Take care to grip with, but not squeeze, the pliers or other tool used to remove a jumper, or the pins on the board may bend or break.



CAUTION!

Risk of explosion if battery is replaced incorrectly or with an incorrect type. Replace the battery only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

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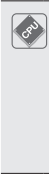


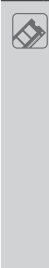


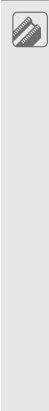
Chapter 1 Hardware Installation

1-1 Installation Precautions

The motherboard/system contain numerous delicate electronic circuits and components which can become damaged as a result of electrostatic discharge (ESD). Prior to installation, carefully read the service guide and follow these procedures:

- Prior to installation, do not remove or break motherboard S/N (Serial Number) sticker or warranty sticker provided by your dealer. These stickers are required for warranty validation.
- Always remove the AC power by unplugging the power cord from the power outlet before installing or removing the motherboard or other hardware components.
- When connecting hardware components to the internal connectors on the motherboard, make sure they are connected tightly and securely.
- When handling the motherboard, avoid touching any metal leads or connectors.
- It is best to wear an electrostatic discharge (ESD) wrist strap when handling electronic components such as a motherboard, CPU or memory. If you do not have an ESD wrist strap, keep your hands dry and first touch a metal object to eliminate static electricity.
- Prior to installing the motherboard, please have it on top of an antistatic pad or within an electrostatic shielding container.
- Before unplugging the power supply cable from the motherboard, make sure the power supply has been turned off.
- Before turning on the power, make sure the power supply voltage has been set according to the local voltage standard.
- Before using the product, please verify that all cables and power connectors of your hardware components are connected.
- To prevent damage to the motherboard, do not allow screws to come in contact with the motherboard circuit or its components.
- Make sure there are no leftover screws or metal components placed on the motherboard or within the computer casing.
- Do not place the computer system on an uneven surface.
- Do not place the computer system in a high-temperature environment.
- Turning on the computer power during the installation process can lead to damage to system components as well as physical harm to the user.
- If you are uncertain about any installation steps or have a problem related to the use of the product, please consult a certified computer technician.

1-2 Product Specifications

	<p>System</p> <ul style="list-style-type: none"> ◆ 2U <p>Dimension</p> <ul style="list-style-type: none"> ◆ 438mm (W) x 87.5mm (H) x 730mm (D)
	<p>CPU</p> <ul style="list-style-type: none"> ◆ AMD EPYC™ 7002 series processor family ◆ Single processor, 7nm technology ◆ Up to 64-core, 128 threads per processor ◆ Fully support 280W <p>Compatible with AMD EPYC™ 7001 series processor family</p>
	<p>Chipset</p> <ul style="list-style-type: none"> ◆ System on Chip
	<p>Hardware-Level Root of Trust Support</p> <ul style="list-style-type: none"> ◆ Supported <p>NOTE! The system will take extra time to boot as it goes through RoT authentication.</p>
	<p>Memory</p> <ul style="list-style-type: none"> ◆ 16 x DIMM slots ◆ DDR4 memory supported only ◆ 8-Channel memory architecture ◆ RDIMM modules up to 128GB supported ◆ LRDIMM modules up to 128GB supported ◆ Memory speed: Up to 3200*/ 2933 MHz <p>- Note: * Follow BIOS setting and memory QVL list if running 3200 Mhz with 2DPC</p>
	<p>LAN</p> <ul style="list-style-type: none"> ◆ 2 x 1GbE LAN ports (1 x Intel® I350-AM2) ◆ 1 x 10/100/1000 management LAN
	<p>Video</p> <ul style="list-style-type: none"> ◆ Integrated in Aspeed® AST2500 ◆ 2D Video Graphic Adapter with PCIe bus interface ◆ 1920x1200@60Hz 32bpp
	<p>Expansion Slot</p> <ul style="list-style-type: none"> ◆ Riser Card CRS2027: <ul style="list-style-type: none"> - 1 x PCIe x8 slot (Gen4 x8), Low profile half-length - 1 x PCIe x8 slot (Gen4 x8), Low profile half-length ◆ Riser Card CRS2225: <ul style="list-style-type: none"> - 1 x PCIe x16 slot (Gen4 x16), Full height half-length - 1 x PCIe x8 slot (Gen4 x8), Full height half-length - 1 x PCIe x16 slot (Gen4 x16), Full height half-length ◆ Riser Card CRS2225: <ul style="list-style-type: none"> - 1 x PCIe x16 slot (Gen4 x16), Full height half-length - 1 x PCIe x8 slot (Gen4 x8), Full height half-length - 1 x PCIe x16 slot (Gen4 x16 or x8, shared with OCP2.0 mezzanine slot), Full height half-length



Expansion Slot (continued)

- ◆ **Internal Riser Card CRS101H:**
 - » **R262-ZA1**
 - 1 x PCIe x16 slot (Gen4 x16), Full height half-length
 - » **R262-ZA2**
 - 1 x PCIe x16 slot (Gen4 x16), Full height half-length, occupied by CNV3134, 4 x NVMe Card
- ◆ 1 x OCP 3.0 mezzanine slot with PCIe Gen4 x16 bandwidth
- ◆ 1 x OCP 2.0 mezzanine slot with PCIe Gen3 x0 or x8 bandwidth, shared with CRS2225



Storage

- ◆ **Front Side:** 12 x 3.5" hot-swappable HDD/SSD bays
 - » **R262-ZA1**
 - *12 x blue HDD/SSD trays compatible with SATA/SAS devices
 - » **R262-ZA2**
 - 4 x green HDD/SSD trays compatible with SATA/SAS/NVMe devices
 - 8 x blue HDD/SSD trays compatible with SATA/SAS devices, enabled by optional SAS Card
- ◆ **Rear Side:** 2 x 2.5" SATA/SAS hot-swappable HDD/SSD bays
- ◆ **SAS card is required to enable the drive bays**
- ◆ **Default Configuration supports:**
 - 4 x 3.5" SATA/SAS drives in front side
 - 2 x 2.5" SATA/SAS drives in rear side
- ◆ Recommended 12Gb/s SAS cards:
 - CRA4448
 - CRA3338
- ◆ 1 x M.2 slot:
 - M-key
 - PCIe Gen4 x4
 - Supports NGFF-2280/22110 cards

* NOTE: 8 x blue HDD/SSD trays are enabled by optional SAS Card








SAS

- ◆ Depends on SAS add-on card



RAID

- ◆ Depends on SAS add-on card

	Internal I/O	<ul style="list-style-type: none"> ◆ 1 x M.2 slot ◆ 1 x USB 3.0 header ◆ 1 x COM header ◆ 1 x TPM header ◆ 1 x OCP 3.0 mezzanine slot ◆ 1 x OCP 2.0 mezzanine slot ◆ 1 x Front panel header ◆ 1 x HDD back plane board header ◆ 1 x PMBus connector ◆ 1 x IPMB connector ◆ 1 x Clear CMOS jumper ◆ 1 x BIOS recovery jumper
	Front I/O	<ul style="list-style-type: none"> ◆ 2 x USB 3.0 ◆ 1 x Power button with LED ◆ 1 x ID button with LED ◆ 1 x NMI button ◆ 1 x Reset button ◆ 2 x LAN activity LEDs ◆ 1 x HDD activity LED ◆ 1 x System status LED
	Rear I/O	<ul style="list-style-type: none"> ◆ 2 x USB 3.0 ◆ 1 x VGA ◆ 2 x RJ45 ◆ 1 x MLAN ◆ 1 x ID button with LED
	Backplane I/O	<p>R262-ZA1</p> <ul style="list-style-type: none"> ◆ Front side_CBP20C5: 12 x SATA/SAS ports ◆ Rear side_CBP2022: 2 x SATA/SAS ports ◆ Speed and bandwidth: SAS 12Gb/s, SATA 6Gb/s <p>R262-ZA2</p> <ul style="list-style-type: none"> ◆ Front side_CBP20C5: 12 x SATA/SAS/NVMe ports ◆ Rear side_CBP2022: 2 x SATA/SAS ports ◆ Speed and bandwidth: SAS 12Gb/s, SATA 6Gb/s, PCIe Gen4 x4
	TPM	<ul style="list-style-type: none"> ◆ 1 x TPM header with SPI interface ◆ Optional TPM2.0 kit: CTM010



System Management

- ◆ Aspeed® AST2500 management controller
- ◆ GIGABYTE Management Console (AMI MegaRAC SP-X) web interface

- ◆ Dashboard
- ◆ JAVA Based Serial Over LAN
- ◆ HTML5 KVM
- ◆ Sensor Monitor (Voltage, RPM, Temperature, CPU Status ...etc.)
- ◆ Sensor Reading History Data
- ◆ FRU Information
- ◆ SEL Log in Linear Storage / Circular Storage Policy
- ◆ Hardware Inventory
- ◆ Fan Profile
- ◆ System Firewall
- ◆ Power Consumption
- ◆ Power Control
- ◆ LDAP / AD / RADIUS Support
- ◆ Backup & Restore Configuration
- ◆ Remote BIOS/BMC/CPLD Update
- ◆ Event Log Filter
- ◆ User Management
- ◆ Media Redirection Settings
- ◆ PAM Order Settings
- ◆ SSL Settings
- ◆ SMTP Settings



Power Supply

R262-ZA1

- ◆ 2 x 1200W redundant PSUs
- ◆ 80 PLUS Platinum

- ◆ AC Input:
 - 100-240V~/ 12-7A, 50-60Hz
- ◆ DC Input:
 - 240Vdc/ 6A

- ◆ DC Output:
 - Max 1000W/ 100-240V~
 - +12V/ 80.5A
 - +12Vsb/ 3A
 - Max 1200W/ 200-240V~ or 240Vdc input
 - +12V/ 97A
 - +12Vsb/ 3A



Power Supply

R262-ZA2

- ◆ 2 x 1600W redundant PSUs
- ◆ 80 PLUS Platinum

- ◆ AC Input:
 - 100-127V~/ 12A, 47-63Hz
 - 200-240V~/ 9.48A, 47-63Hz

- ◆ DC Output:
 - Max 1000W/ 100-127V
 - +12V/ 82A
 - +12Vsb/ 2.1A
 - Max 1600W/ 200-240V
 - +12V/ 132A
 - +12Vsb/ 2.1A



Environment

Ambient Temperature

- ◆ Operating temperature: 10°C to 35°C
- ◆ Operating humidity: 8-80% (non-condensing)

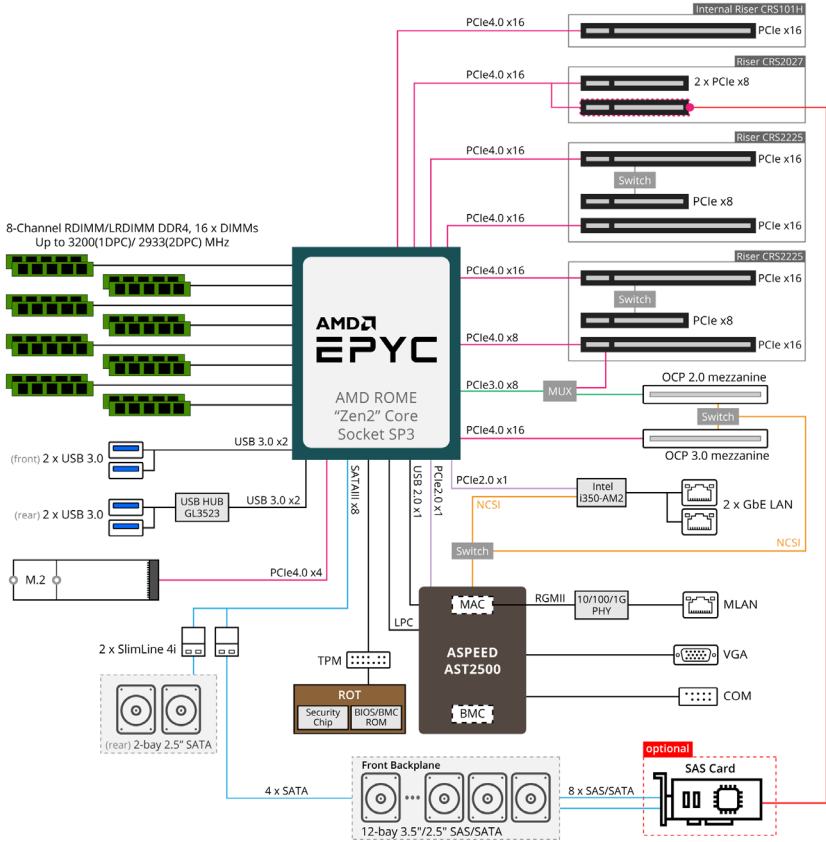
Relative Humidity

- ◆ Non-operating temperature: -40°C to 60°C
- ◆ Non-operating humidity: 20%-95% (non-condensing)

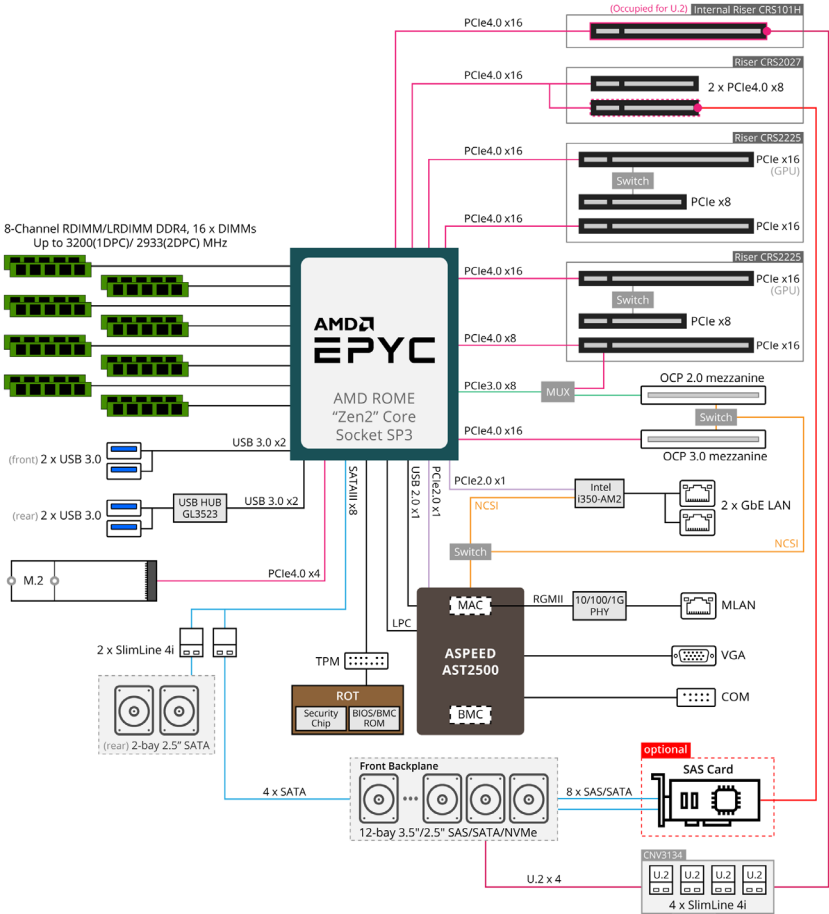
* We reserve the right to make any changes to the product specifications and product-related information without prior notice.

1-3 System Block Diagram

R262-ZA1

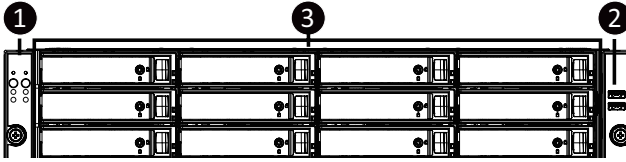


R262-ZA2



Chapter 2 System Appearance

2-1 Front View

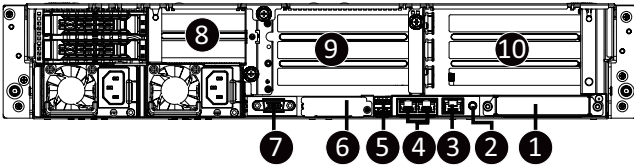


No.	Description
1.	Front Panel LEDs and Buttons
2.	Front USB 3.0 Ports
3.	3.5"/2.5" HDD Bays
NOTE! Green Latches Support NVMe.	



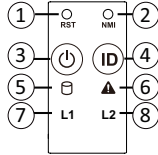
- Please Go to Chapter **2-3 Front Panel LEDs and Buttons** for detail description of function LEDs.

2-2 Rear View



No.	Description
1.	Mezzanine Card Slot (Option/OCP 3.0/SFF)
2.	ID Button with LED
3.	10/100/1000 Server Management LAN Port
4.	1GbE LAN Port x 2
5.	USB 3.0 Port x 2
6.	Mezzanine Card Slot (Option/OCP 2.0)
7.	VGA Port
8.	Low-Profile PCIe Card Slot
9.	Full-Height PCIe Card Slot
10.	Full-Height PCIe Card Slot

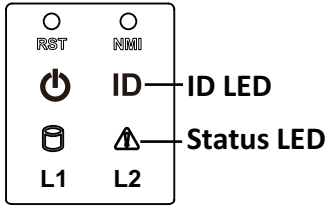
2-3 Front Panel LEDs and Buttons



No.	Name	Color	Status	Description
1.	Reset Button	--	--	Press the button to reset the system.
2.	NMI button	--	--	Press the button server generates a NMI to the processor if the multiple-bit ECC errors occur, which effectively halt the server.
3.	Power button with LED	Green	On	Indicates the system is powered on.
		Green	Blink	System is in ACPI S1 state (sleep mode).
		N/A	Off	<ul style="list-style-type: none"> System is not powered on or in ACPI S5 state (power off) System is in ACPI S4 state (hibernate mode)
4.	ID Button			This LED represents the RoT function LED behavior. Please see the following section for detail LED behavior.
5.	HDD Status LED	Green	On	Indicates locating the HDD.
			Blink	Indicates accessing the HDD.
		Amber	On	Indicates HDD error.
		Green/Amber	Blink	Indicates HDD rebuilding.
		N/A	Off	Indicates no HDD access or no HDD error.
6.	System Status LED			This LED represents the RoT function LED behavior. Please see the following section for detail LED behavior.
7/8.	LAN 1/2 Active/Link LEDs	Green	On	Indicates a link between the system and the network or no access.
		Green	Blink	Indicates data trasmission or receiving is occuring.
		N/A	Off	Indicates no data transmission or receiving is occuring.

(Note) If your server features Dual BIOS function, please see the following section for detail LED behavior.

2-3-1 RoT LEDs



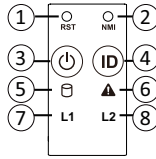
LED on Front panel ^(Note5)		
	ID LED	Status LED
EC Firmware (FW) Authentication fail or not exit		
EC FW is broken or not exit ^(Note1)	OFF	OFF
Authenticating/Recovering BMC/BIOS Images		
Authenticating Images	OFF	OFF
Recovering BMC Active Flash	Blinks Blue 4 times per second	Blinks Green 4 times per second
Recovering BIOS Active Flash	Blinks Blue 4 times per second	Blinks Green 4 times per second
Authentication (AUTH) Pass		
Recovering BIOS Active Flash	OFF	OFF
BMC : AUTH pass after doing recovery	OFF	OFF
BIOS : AUTH pass after doing recovery	OFF	OFF
BMC : AUTH pass	OFF	OFF
BIOS : AUTH pass after doing recovery	OFF	OFF
Active Flash Authentication (AUTH) Fail		
BMC : AUTH Fail ^(Note2)	Blinks Blue 1 time per second	Blinks Green 1 time per second

BIOS : AUTH fail^(Note2)	Blinks Blue 1 time per second	Blinks Amber 1 time per second
BMC : AUTH fail after doing recovery^(Note3)	Blinks Blue 2 times per second [ON OFF OFF]	Blinks Green 2 times per second [ON OFF OFF]
BIOS : AUTH fail after doing recovery^(Note3)	Blinks Blue 2 times per second [ON OFF OFF]	Blinks Amber 2 times per second [ON OFF OFF]
Backup Flash Authentication Fail^(Note4)		
BMC : AUTH fail	Blinks Blue 2 times per second [ON OFF ON OFF]	Blinks Green 2 times per second [ON OFF ON OFF]
BIOS : AUTH fail	Blinks Blue 2 times per second [ON OFF ON OFF]	Blinks Amber 2 times per second [ON OFF ON OFF]

NOTE!

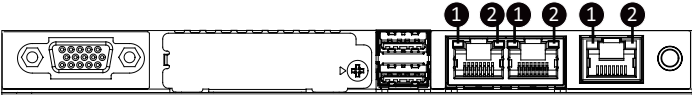
1. EC FW is broken or not exited result in Microchip CEC1702 cannot load EC FW for authentication.
2. (1) Authentication fail include below scenarios
Configuration table is missing or modified
Public key is missing or modified
Protected area or signature is modified
Flash empty
3. If active flash is still authentication failed after recovery sequence, Microchip CEC1702 stop the process and showing LED behavior.
4. If backup flash authentication is failed cause by configuration table, public key or protected area is broken. Microchip CEC1702 stop the process and showing LED behavior.
5. Front panel LED is controlled by BMC or Microchip CEC1702. Once Microchip CEC1702 is working(Auth or recovery), the front panel LED is controlled by Microchip CEC1702 and vice versa.

2-3-2 LEDs Behavior for Dual BIOS Model



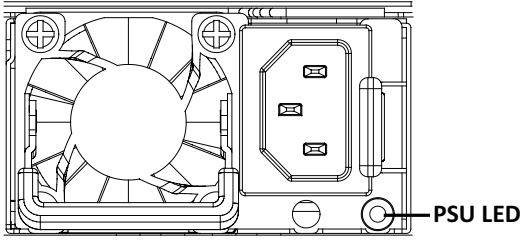
No.	Name	Color	Status	Description
1.	Reset Button			Press the button to reset the system.
2.	NMI button			Press the button server generates a NMI to the processor if the multiple-bit ECC errors occur, which effectively halt the server.
3.	Power button with LED	Green	On	System is powered on
		Green	Blink	System is in ACPI S1 state (sleep mode)
		N/A	Off	<ul style="list-style-type: none"> System is not powered on or in ACPI S5 state (power off) System is in ACPI S4 state (hibernate mode)
4.	ID Button ^(Note)			Press the button to activate system identification
5.	HDD Status LED	Green	On	HDD locate
			Blink	HDD access
		Amber	On	HDD fault
			Blink	HDD rebuilding
		N/A	Off	No HDD access or no HDD fault.
6.	System Status LED ^(Note)	Green	Solid On	System is operating normally.
			Solid On	Critical condition, may indicate: System fan failure System temperature
		Amber	Blink	Non-critical condition, may indicate: Redundant power module failure Temperature and voltage issue Chassis intrusion
			N/A	Off
7/8.	LAN 1/2 Active/Link LEDs	Green	Solid On	Link between system and network or no access.
		Green	Blink	Data trasmission or receiving is occuring
		N/A	Off	No data transmission or receiving is occuring

2-4 Rear System LAN LEDs



No.	Name	Color	Status	Description
1.	1GbE Speed LED	Yellow	On	1 Gbps data rate
		Green	On	100 Mbps data rate
		N/A	Off	10 Mbps data rate
2.	1GbE Link/ Activity LED	Green	On	Link between system and network or no access
			Blink	Data transmission or receiving is occurring
		N/A	Off	No data transmission or receiving is occurring

2-5 Power Supply Unit (PSU) LED



State	Description
OFF	No AC power to all power supplies
0.5Hz Green Blinking	AC present / only standby on / Cold redundant mode
2Hz Green Blinking	Power supply firmware updating mode
Amber	AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power
	Power supply critical event causing shut down: failure, OCP, OVP, fan failure and UVP
0.5Hz Amber Blinking	Power supply warning events where the power supply continues to operate: high temp, high power, high current and slow fan

2-6 Hard Disk Drive LEDs



RAID SKU		LED1	Locate	HDD Fault	Rebuilding	HDD Access	HDD Present (No Access)
No RAID configuration (via PCH, HBA)	Disk LED (LED on Back Panel)	Green	ON(*1)	OFF		BLINK (*2)	OFF
		Amber	OFF	OFF		OFF	OFF
	Removed HDD Slot (LED on Back Panel)	Green	ON(*1)	OFF		--	--
		Amber	OFF	OFF		--	--
RAID configuration (via HW RAID Card or SW RAID Card)	Disk LED	Green	ON	OFF		BLINK (*2)	OFF
		Amber	OFF	ON	(Low Speed: 2 Hz)	OFF	OFF
	Removed HDD Slot	Green	ON(*1)	OFF	(*3)	--	--
		Amber	OFF	ON	(*3)	--	--

LED 2	HDD Present	No HDD
Green	ON	OFF

NOTE:

*1: Depends on HBA/Utility Spec.

*2: Blink cycle depends on HDD's activity signal.

*3: If HDD is pulled out during rebuilding, the disk status of this HDD is regarded as faulty.

Chapter 3 System Hardware Installation



Pre-installation Instructions

Computer components and electronic circuit boards can be damaged by electrostatic discharge. Working on computers that are still connected to a power supply can be extremely dangerous. Follow the simple guidelines below to avoid damage to your computer or injury to yourself.

- Always disconnect the computer from the power outlet whenever you are working inside the computer case.
- If possible, wear a grounded wrist strap when you are working inside the computer case. Alternatively, discharge any static electricity by touching the bare metal system of the computer case, or the bare metal body of any other grounded appliance.
- Hold electronic circuit boards by the edges only. Do not touch the components on the board unless it is necessary to do so. Do not flex or stress the circuit board.
- Leave all components inside the static-proof packaging until you are ready to use the component for the installation.

3-1 Removing Chassis Cover

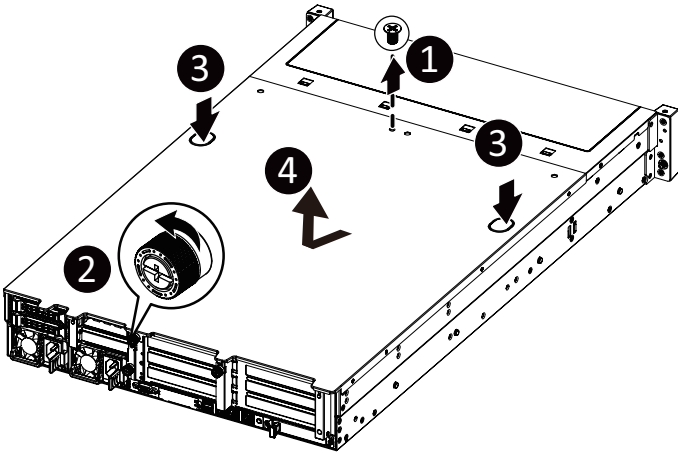


Before you remove or install the system cover

- Make sure the system is not turned on or connected to AC power.

Follow these instructions to remove the chassis cover:

1. Remove the screw securing the chassis cover.
2. Loosen the thumbscrew securing the chassis cover.
3. Push down the indentations located on the sides of the chassis cover.
4. Slide the cover forward towards the rear of the system and then remove the cover in the direction indicated by the arrow.
5. To reinstall the chassis cover reverse steps 1-4.

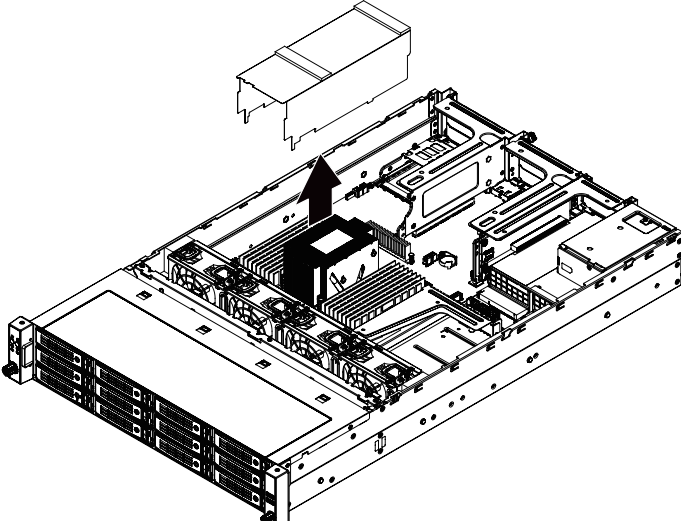


3-2 Removing and Installing the Fan Duct

R262-ZA1

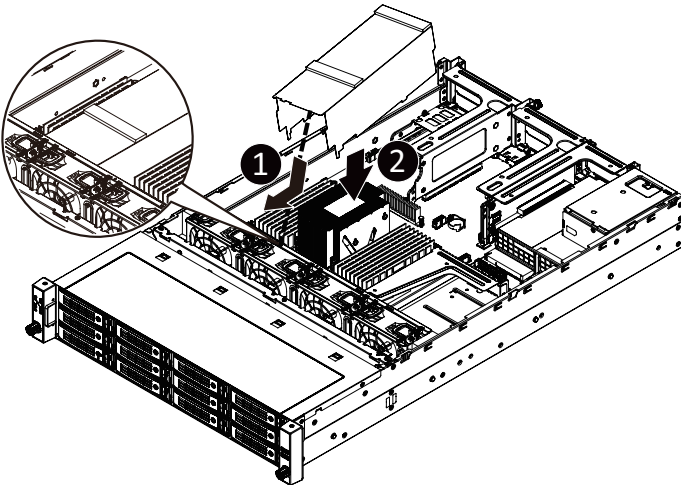
Follow these instructions to remove the fan duct:

1. Lift up to remove the two fan ducts



Follow these instructions to install the fan duct:

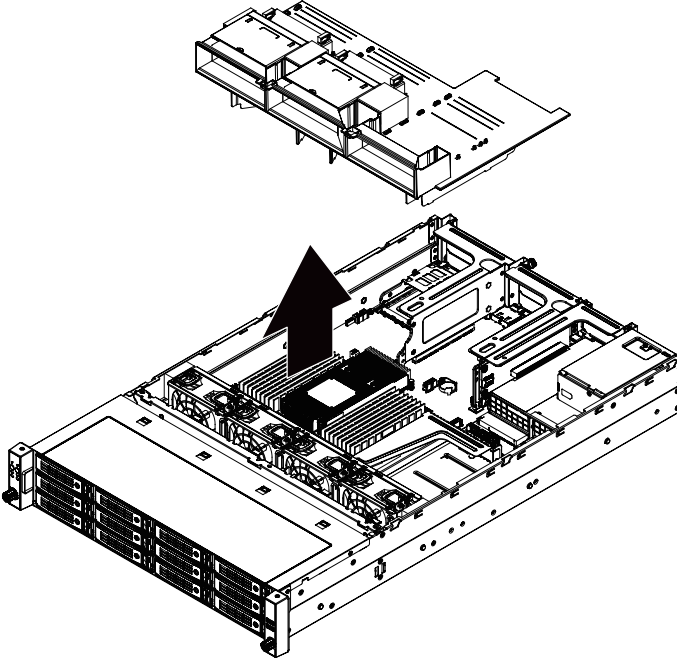
1. Tilt the fan duct, align the fan duct with the guiding groove and fix the front side of fan duct in the flange under the fan wall.
2. Push down the fan duct into chassis until its firmly seats.



R262-ZA2

Follow these instructions to remove the fan duct:

1. Lift up to remove the two fan ducts
2. To install the fan duct, align the fan duct with the guiding groove. Push down the fan duct into chassis until its firmly seats.

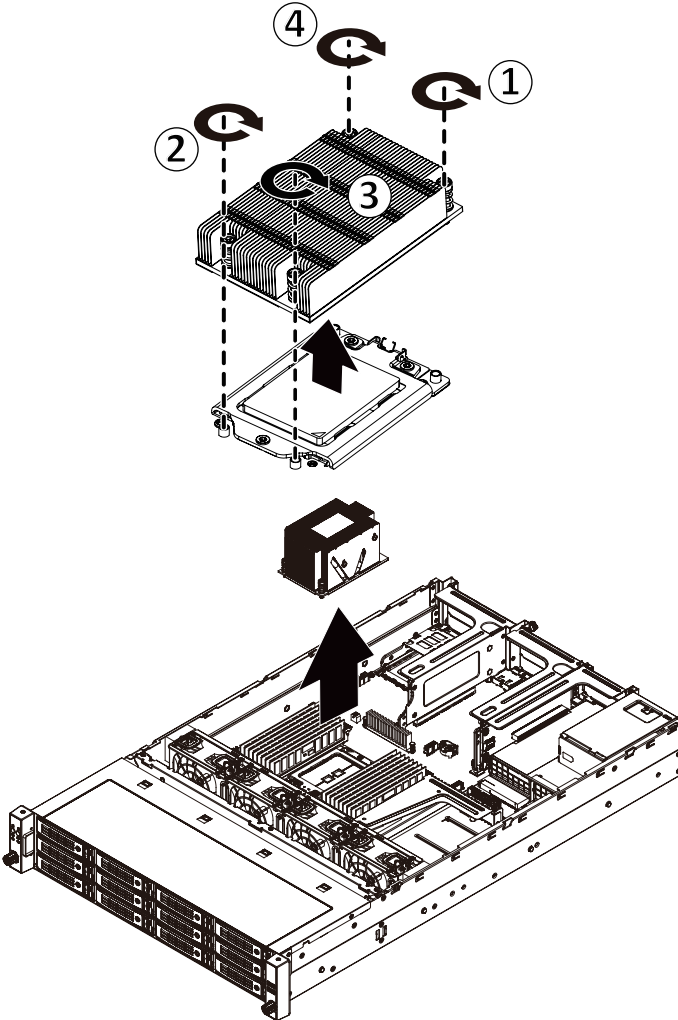


3-3 Removing the Heat Sink

R262-ZA1

Follow these instructions to remove/install the fan duct:

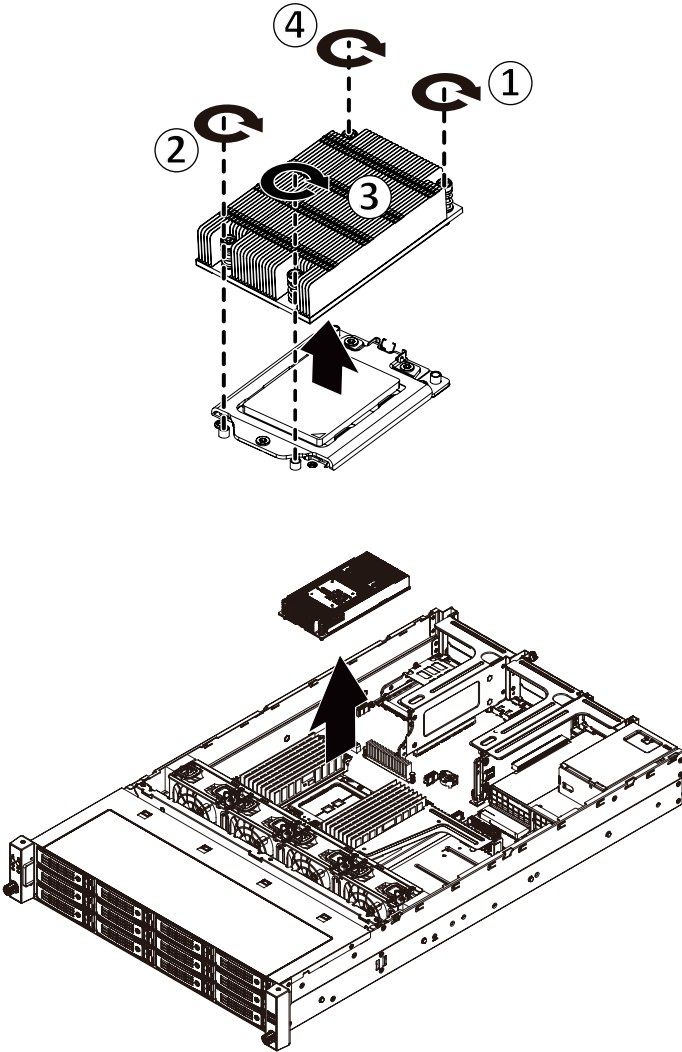
1. Loosen the captive screws securing the heatsink in place in reverse order (4→3→2→1).
2. Lift and remove the heat sink from the system.
3. To reinstall the heat sink reverse steps 1-2 while ensuring that you tighten the captive screws in sequential order (1→2→3→4) as seen in the image below.



R262-ZA2

Follow these instructions to remove/install the fan duct:

1. Loosen the captive screws securing the heatsink in place in reverse order (4→3→2→1).
2. Lift and remove the heat sink from the system.
3. To reinstall the heat sink reverse steps 1-2 while ensuring that you tighten the captive screws in sequential order (1→2→3→4) as seen in the image below.



3-4 Installing the CPU



Read the following guidelines before you begin to install the CPU:

- Make sure that the motherboard supports the CPU.
- Always turn off the computer and unplug the power cord from the power outlet before installing the CPU to prevent hardware damage.
- Unplug all cables from the power outlets.
- Disconnect all telecommunication cables from their ports.
- Place the system unit on a flat and stable surface.
- Open the system according to the instructions.



WARNING!

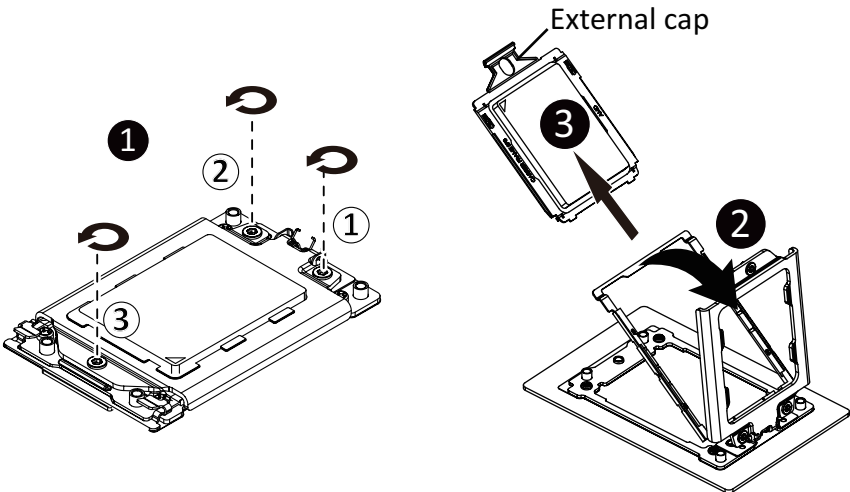
Failure to properly turn off the server before you start installing components may cause serious damage. Do not attempt the procedures described in the following sections unless you are a qualified service technician.

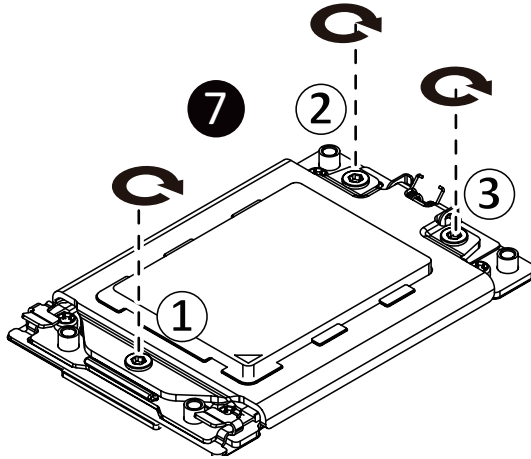
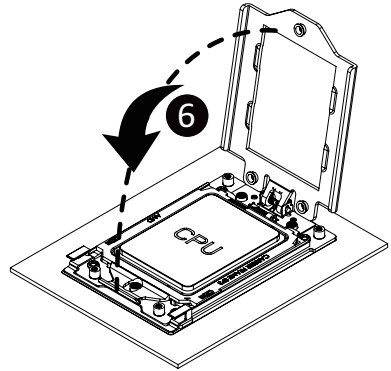
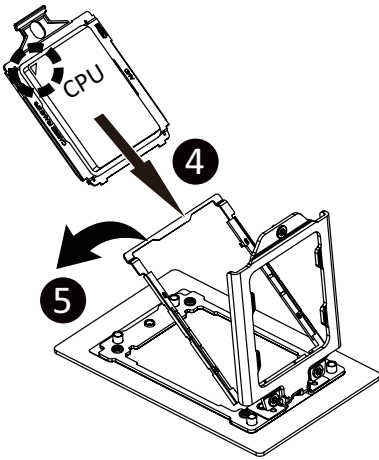
Follow these instructions to install the CPU:

1. Loosen the three captive screws securing the CPU cover in sequential order (1 → 2 → 3).
2. Flip open the CPU cover.
3. Remove the CPU carrier from the CPU frame using the handle on the CPU carrier.
4. Using the handle on the CPU carrier insert the new CPU carrier with CPU installed into the CPU frame.

NOTE: Ensure the CPU is installed in the CPU carrier in the correct orientation, with the triangle on the CPU aligned to the top left corner of the CPU carrier.

5. Flip the CPU frame with CPU installed into place in the CPU socket.
6. Flip the CPU cover into place over the CPU socket.
7. Tighten the CPU cover screws in sequential order (1 → 2 → 3) to secure the CPU cover in place.





NOTE!

- When installing the heatsink to CPU, use PHILLIPS #2 driver to tighten 4 captive nuts in sequence as 1-4.
- The screw tightening torque: $10 \pm 0.5 \text{ kgf-cm}$ ($8.8 \pm 0.4 \text{ lbf-in}$)

3-5 Installing the Memory

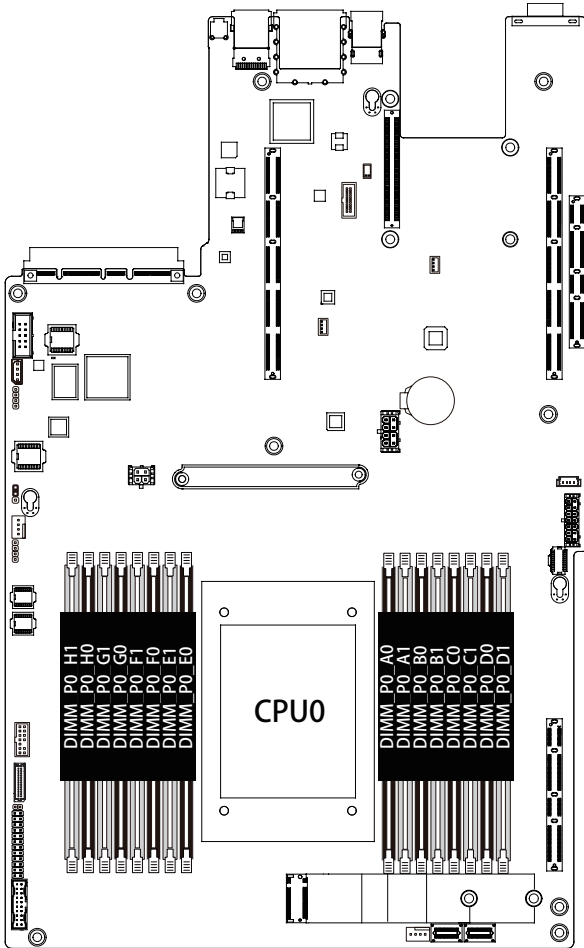


Read the following guidelines before you begin to install the memory:

- Make sure that the motherboard supports the memory. It is recommended that memory of the same capacity, brand, speed, and chips be used.
- Always turn off the computer and unplug the power cord from the power outlet before installing the memory to prevent hardware damage.
- Memory modules have a foolproof design. A memory module can be installed in only one direction. If you are unable to insert the memory, switch the direction.

3-5-1 Eight Channel Memory Configuration

This motherboard provides 16 DDR4 memory slots and supports Eight Channel Technology. After the memory is installed, the BIOS will automatically detect the specifications and capacity of the memory.



3-5-2 Installing the Memory

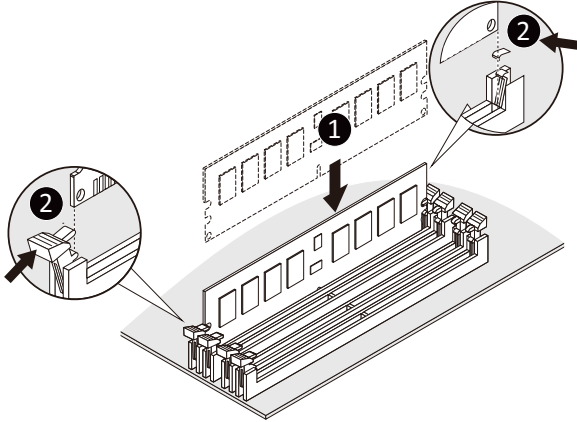


Before installing a memory module, make sure to turn off the computer and unplug the power cord from the power outlet to prevent damage to the memory module.

Be sure to install DDR4 DIMMs on this motherboard.

Follow these instructions to install the Memory:

1. Insert the DIMM memory module vertically into the DIMM slot, and push it down.
2. Close the plastic clip at both edges of the DIMM slots to lock the DIMM module.
3. Reverse the installation steps when you want to remove the DIMM module.



3-5-3 DIMM Population Table

RDIMM Maximum Frequency Supported Table

DIMMs Populated	DIMM		Frequency (MT/s)
	1R	2R 2DR	1.2V
1	1	--	3200
	--	1	3200
2	2	--	2933
	1	1	2933
	--	2	2933

LRDIMM Maximum Frequency Supported Table

DIMMs Populated	DIMM		Frequency (MT/s)
	2S2R 2S4R	4DR	1.2V
1	1	--	3200
	--	1	3200
2	2	--	2933
	1	1	Not Supported
	--	2	2933

3DS RDIMM Maximum Frequency Supported Table

DIMMs Populated	DIMM	Frequency (MT/s)
	2S2R 2S4R	1.2V
1	1	2933
2	2	2666

NOTE!

- 1R: 1 package rank of SDP DRAMs
- 2R: 2 package rank of SDP DRAMs
- 2DR: 2 package rank of DDP DRAMs
- 4DR: 4 package rank of DDP DRAMs
- 2S2R/2S4R/2S8R: 2 package rank of 2/4/8 high 3DS DRAMs
- When only one DIMM is used, it must be populated in memory slot DIMM1.

3-6 Installing the PCI Expansion Card



- Voltages can be present within the server whenever an AC power source is connected. This voltage is present even when the main power switch is in the off position. Ensure that the system is powered-down and all power sources have been disconnected from the server prior to installing a PCIe card.
- Failure to observe these warnings could result in personal injury or damage to equipment.

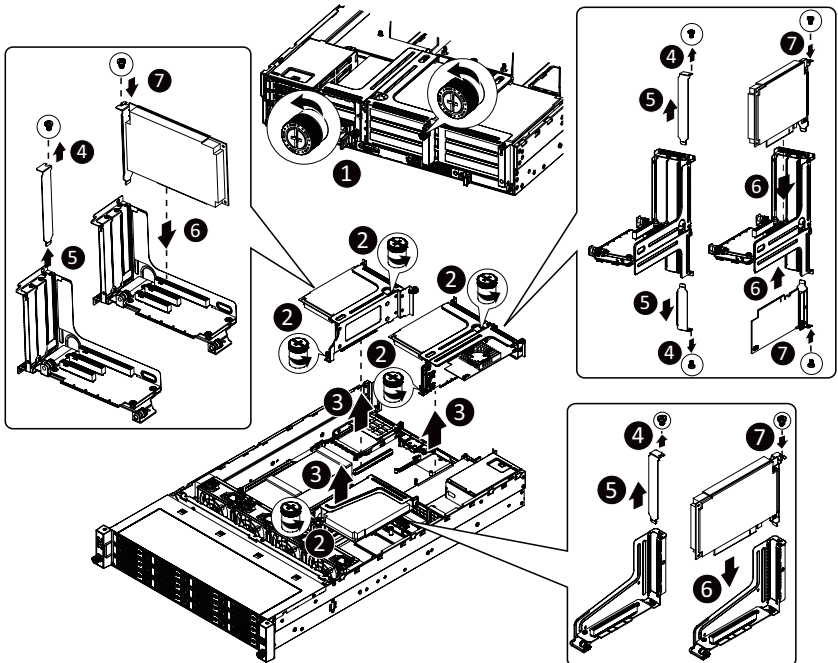


- The PCIe riser assembly does not include a riser card or any cabling as standard. To install a PCIe card, a riser card must be installed.

R262-ZA1

Follow these instructions to PCI Expansion card:

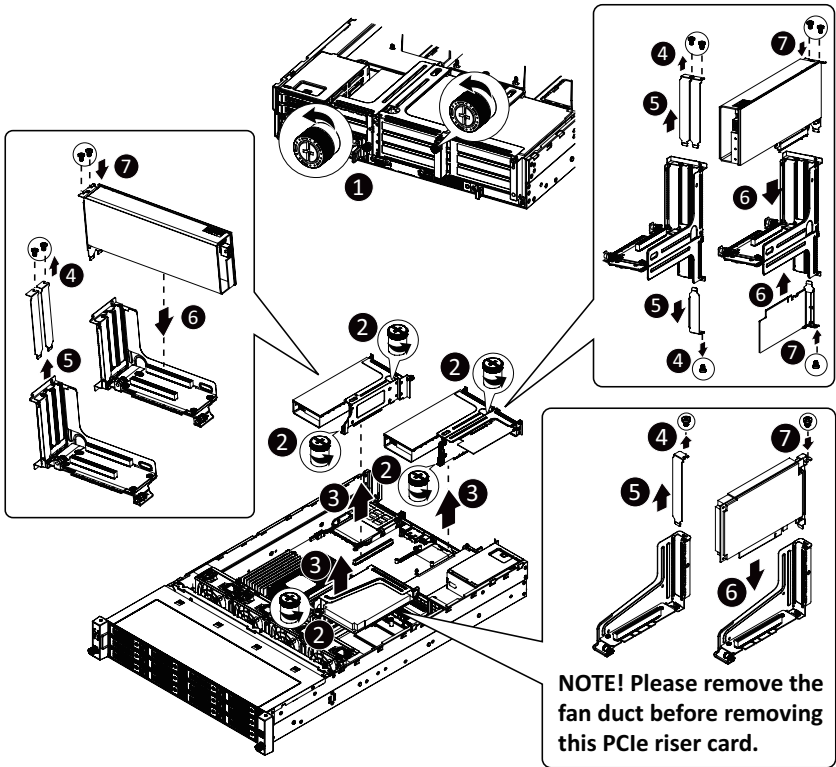
1. Loosen the thumbscrew on the back cover.
2. Loosen the thumbscrew securing the riser bracket.
3. Lift up the riser bracket out of system.
4. Remove the screw securing the slot cover from the riser bracket.
5. Remove the slot covers from the riser bracket.
6. Orient the PCIe card with the riser guide slot and push in the direction of the arrow until the PCIe card sits in the PCIe card connector.
7. Secure the PCIe card with the screw.
8. Reverse the previous steps to install the riser bracket.



R262-ZA2

Follow these instructions to PCI Expansion card:

1. Loosen the thumbscrew on the back cover.
2. Loosen the thumbscrew securing the riser bracket.
3. Lift up the riser bracket out of system.
4. Remove the screw securing the slot cover from the riser bracket.
5. Remove the slot covers from the riser bracket.
6. Orient the PCIe card with the riser guide side and push in the direction of the arrow until the PCIe card sits in the PCIe card connector.
7. Secure the PCIe card with the screw.
8. Reverse the previous steps to install the riser bracket.



3-7 Installing the Mezzanine Card

3-7-1 OCP 3.0

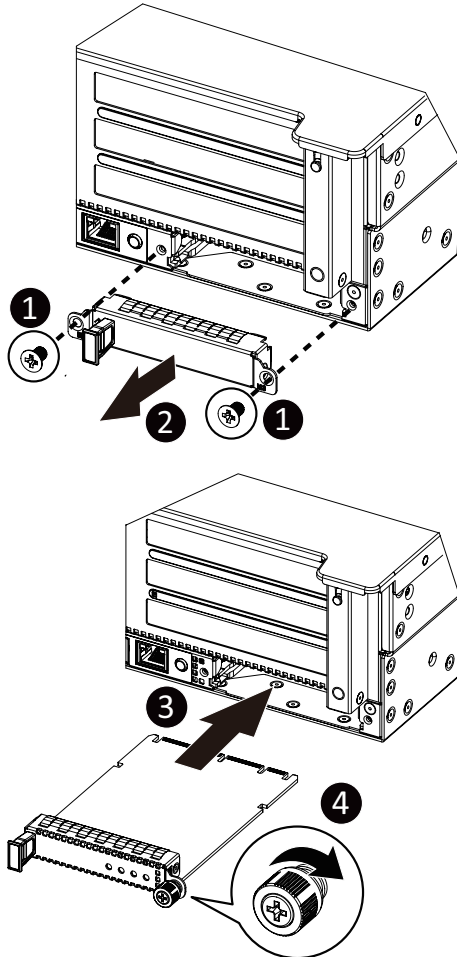


Use of the following type of OCP 3.0 NIC is recommended:

- OCP 3.0 SFF with Pull Tab
- OCP 3.0 SFF with Ejector Latch

Follow these instructions to install an OCP 3.0 mezzanine card:

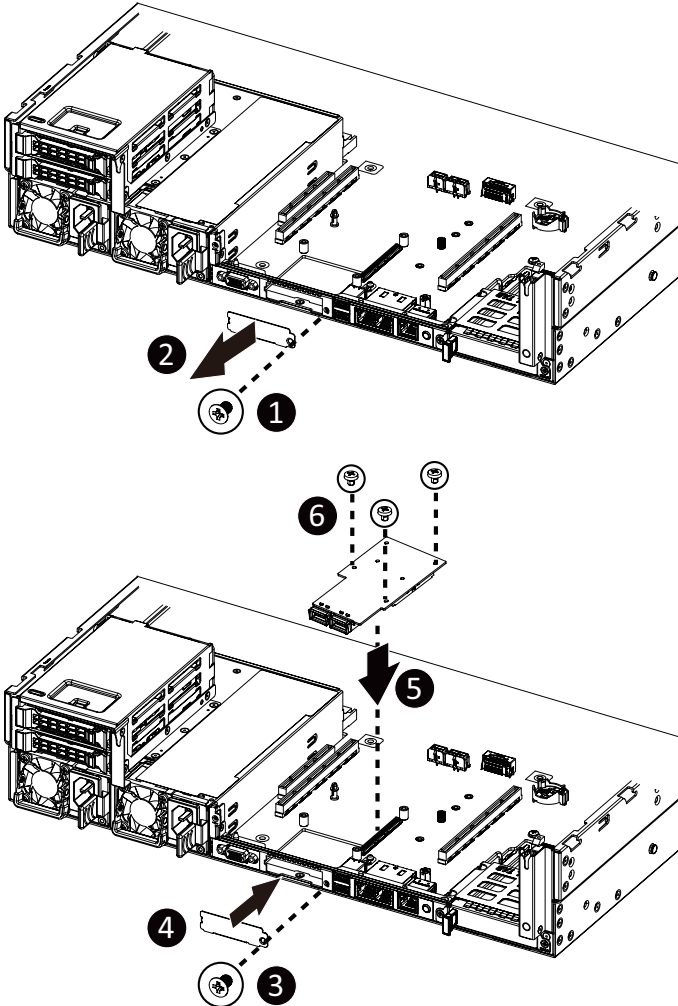
1. Remove the two screws securing the mezzanine card slot cover.
2. Remove the slot cover from the system.
3. Insert the OCP 3.0 mezzanine card into the card slot ensuring that the card is firmly connected to the connector on the motherboard.
4. Tighten the thumbnail screw to secure the OCP 3.0 mezzanine card in place.
5. Reverse the previous steps to replace the OCP 3.0 mezzanine card.



3-7-2 OCP 2.0

Follow these instructions to install an OCP 2.0 mezzanine card:

1. Remove the screw securing the mezzanine card slot cover.
2. Remove the slot cover from the system.
3. Install the OCP 2.0 slot cover to the system
4. Secure the OCP 2.0 slot cover with the screw.
5. Insert the OCP 2.0 mezzanine card into the compartment ensuring that the card is firmly connected to the connector on the motherboard.
6. Secure the OCP 2.0 mezzanine card into the system with three screws.
7. Reverse previous steps to replace the OCP 2.0 mezzanine card.



3-8 Installing the Hard Disk Drive

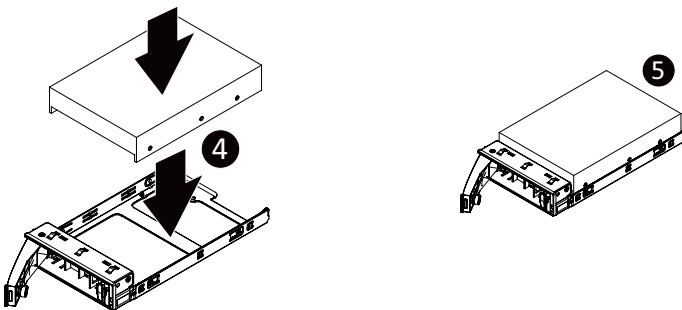
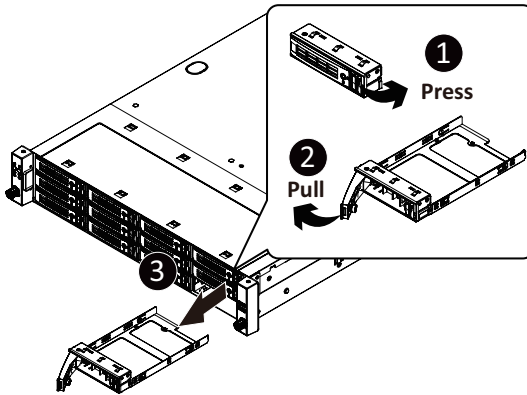


Read the following guidelines before you begin to install the HDD:

- Take note of the drive tray orientation before sliding it out.
- The tray will not fit back into the bay if inserted incorrectly.
- Make sure that the HDD is connected to the HDD connector on the backplane.

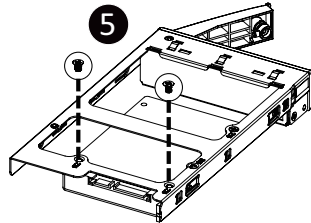
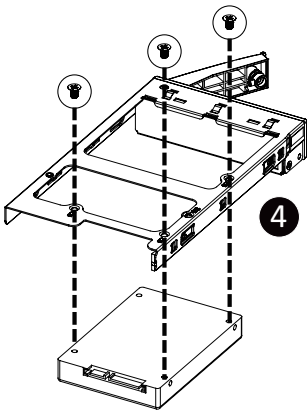
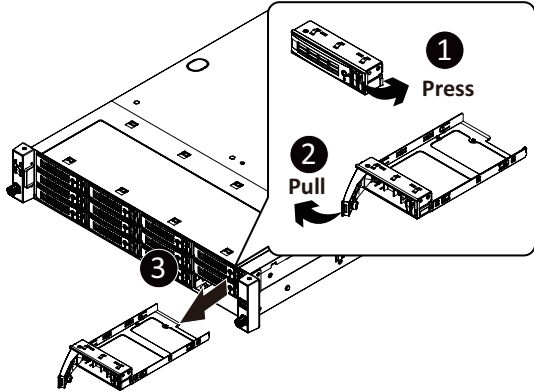
Follow these instructions to install a 3.5" HDD:

1. Press the release button.
2. Extend the locking lever.
3. Pull the locking lever in the direction indicated to remove the 3.5" HDD tray.
4. Slide the hard disk drive into the HDD tray.
5. Reinsert the HDD tray into the slot and close the locking lever.



Follow these instructions to install a 2.5" HDD:

1. Press the release button.
2. Extend the locking lever.
3. Pull the locking lever in the direction indicated to remove the 2.5" HDD tray.
4. Install 3 screws to secure the hard drive to the HDD tray.
5. Install 2 screws to secure the hard drive to the HDD tray.
6. Reinsert the HDD tray into the slot and close the locking lever.



3-9 Installing the M.2 Device and Heat Sink



WARNING:

Installation of the thermal pad over the M.2 device is required when installing an M.2 device. Lack of the thermal pad may result in the system overheating and throttle the system performance.

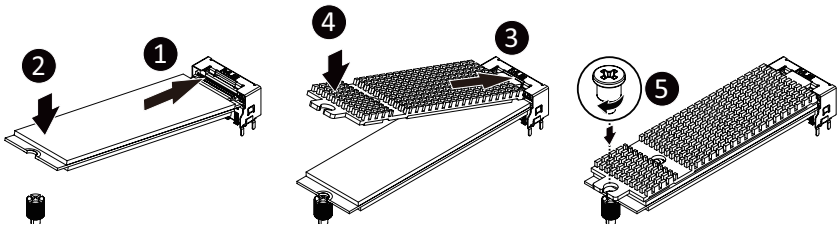


CAUTION

The position of the stand-off screw will depend on the size of the M.2 device. The stand-off screw is pre-installed for 22110 cards as standard. Refer to the size of the M.2 device and change the position of the stand-off screw accordingly.

Follow these instructions to install the M.2 device and heat sink:

1. Insert the M.2 device into the M.2 connector.
2. Press down on the M.2 device.
3. Install the thermal pad of the M.2 device to the M.2 device.
4. Press down on the thermal pad.
5. Secure the M.2 device and its thermal pad to the motherboard with a single screw.
6. Reverse steps 1-4 to remove the M.2 device.



3-10 Replacing the Fan Assembly

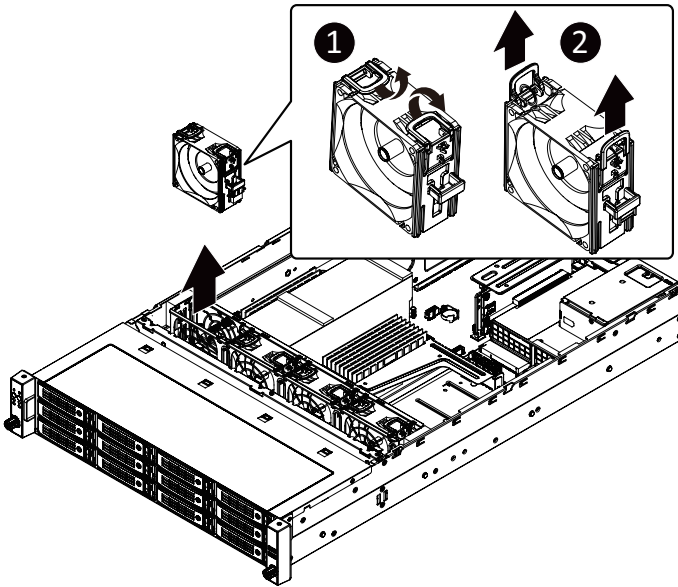


- Voltages can be present within the server whenever an AC power source is connected. This voltage is present even when the main power switch is in the off position. Ensure that the system is powered-down and all power sources have been disconnected from the server prior to replacing a system fan.

Failure to observe these warnings could result in personal injury or damage to equipment.

Follow these instructions to replace the fan assembly:

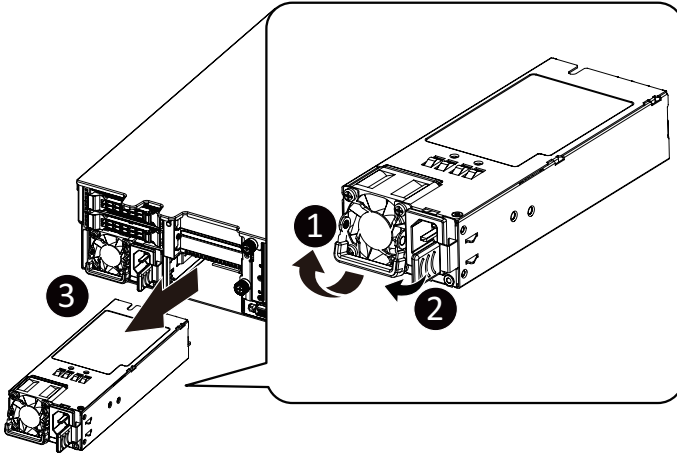
1. Pull outward the fan ear.
2. Lift up the fan assembly from the chassis.
3. Reverse the previous steps to install the replacement fan assembly.



3-11 Replacing the Power Supply

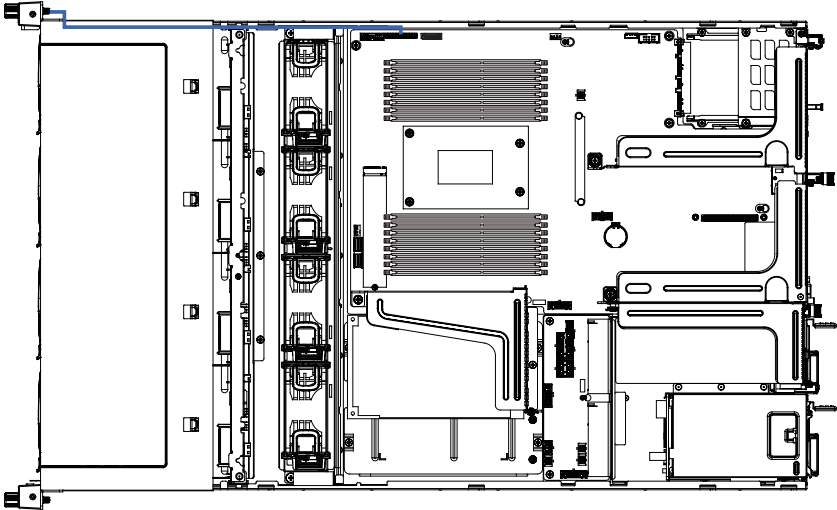
Follow these instructions to replace the power supply:

1. Press the retaining clip on the right side of the power supply along the direction of the arrow.
2. Pull out the power supply handle at the same time and pull out the power supply.
3. Insert the replacement power supply firmly into the chassis. Connect the AC power cord to the replacement power supply.

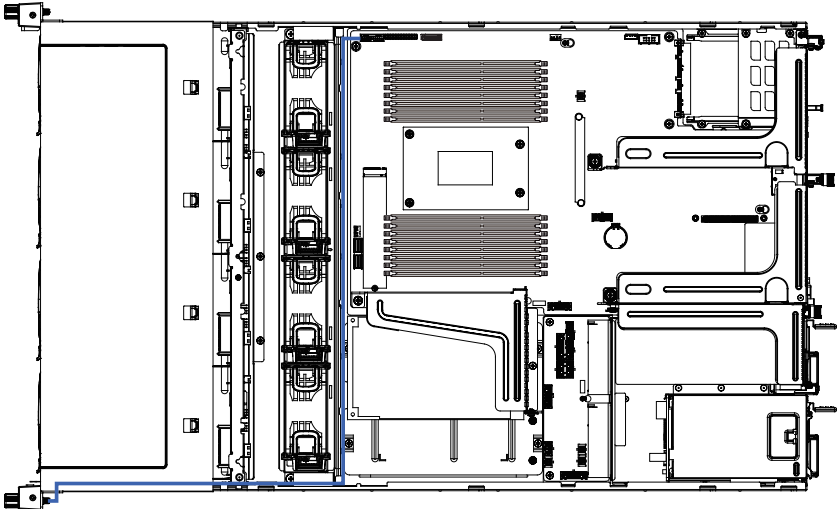


3-12 Cable Routing

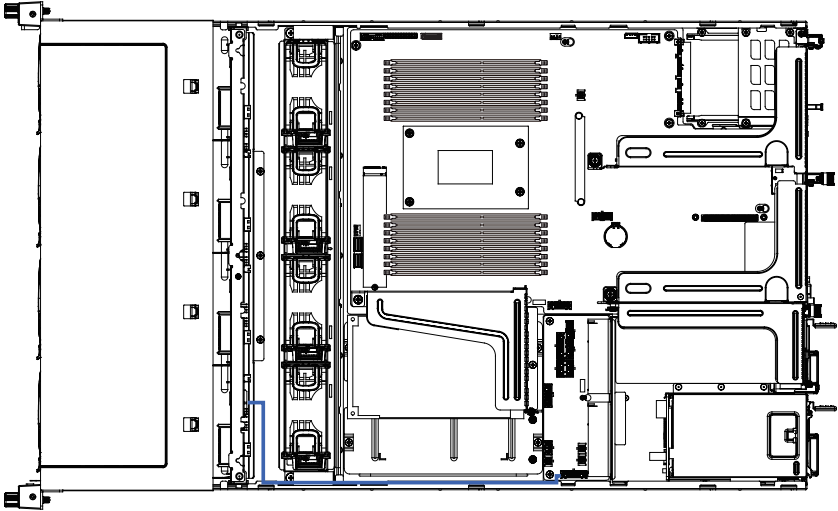
Front Switch Cable/Front LED Cable



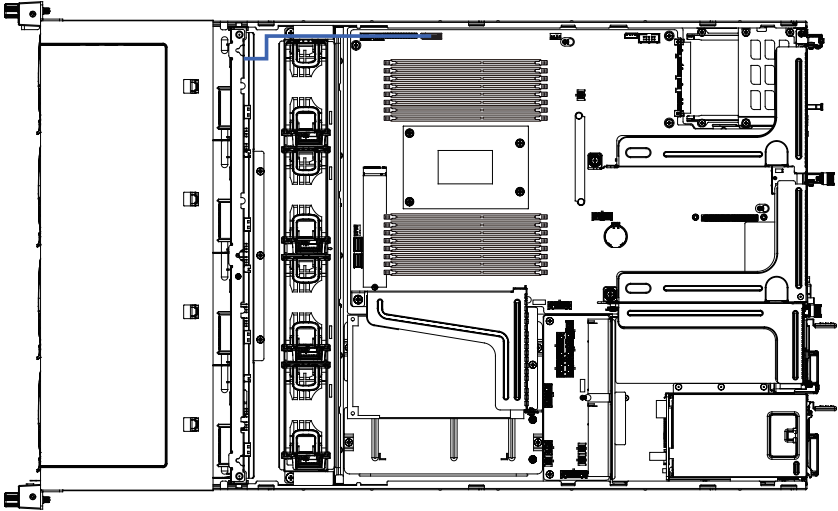
Front Panel USB 3.0 Cable



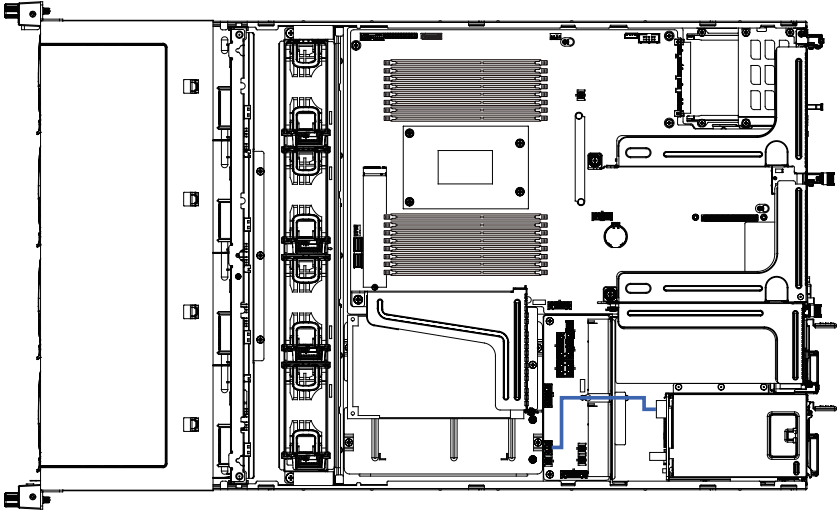
Front HDD Backplane Board Power Cable



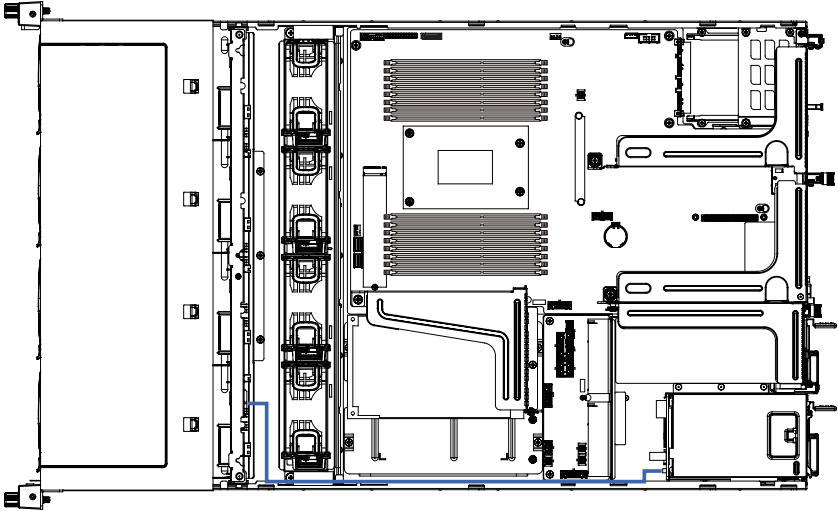
Front HDD Backplane Board Signal Cable



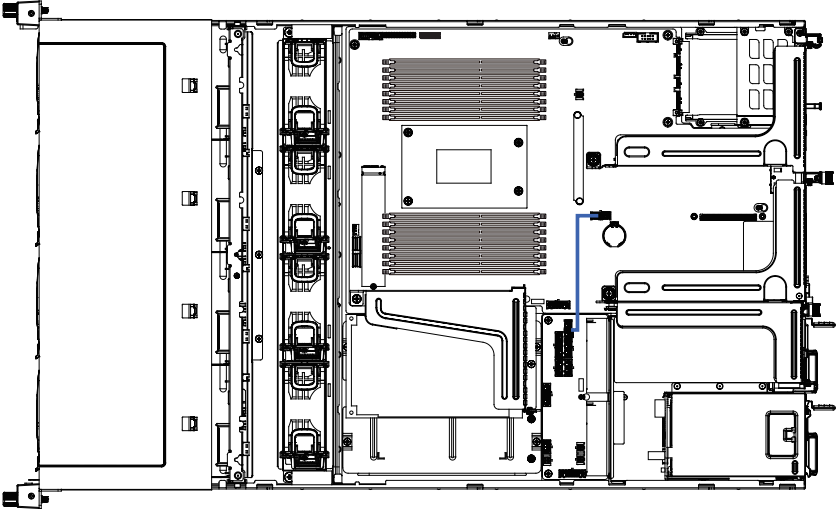
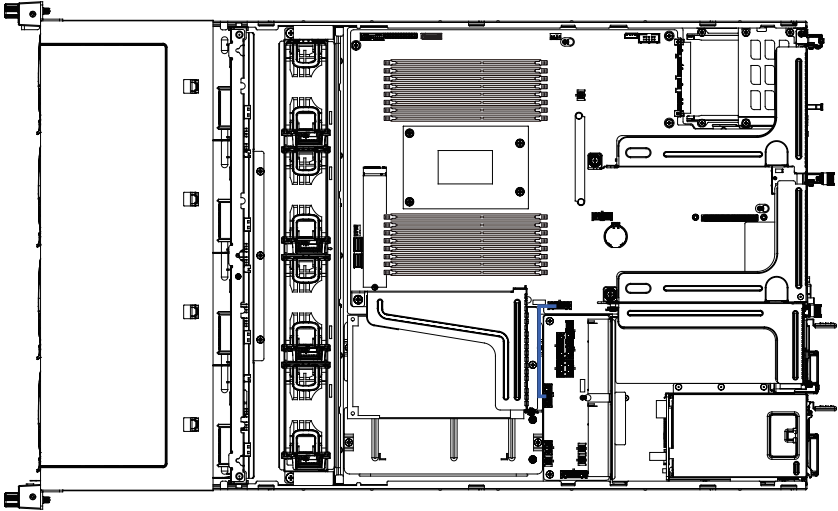
Rear HDD Backplane Board Power Cable



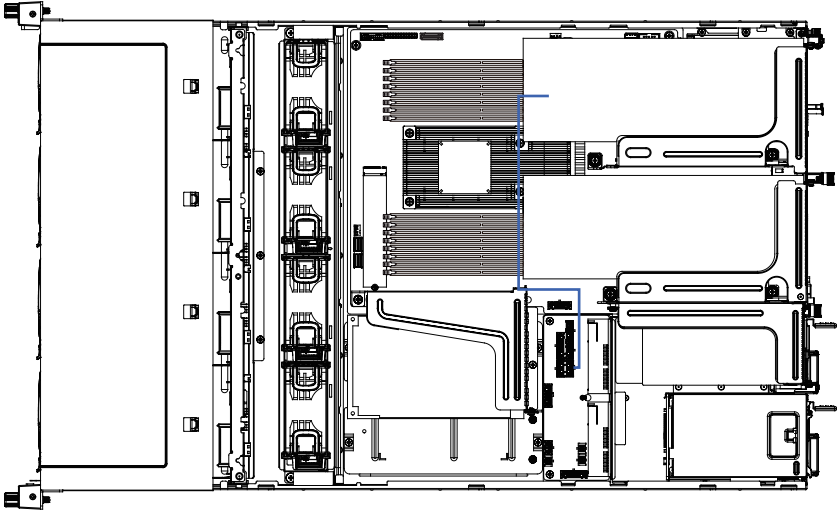
Rear HDD Backplane Board Signal Cable



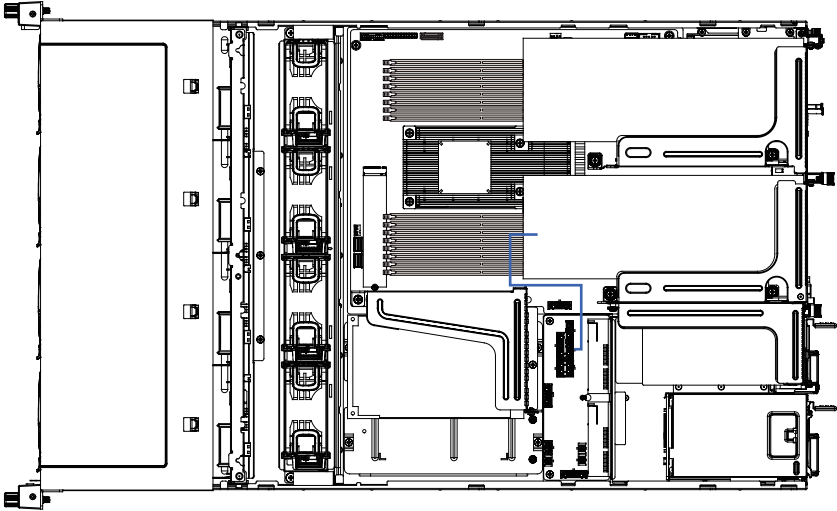
ATX Power Cable



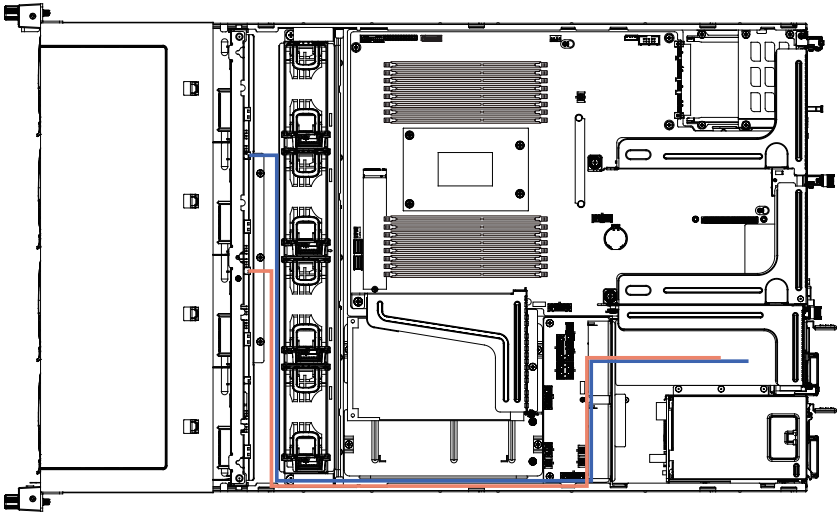
GPU Card#1 Power Cable (for R262-ZA2 only)



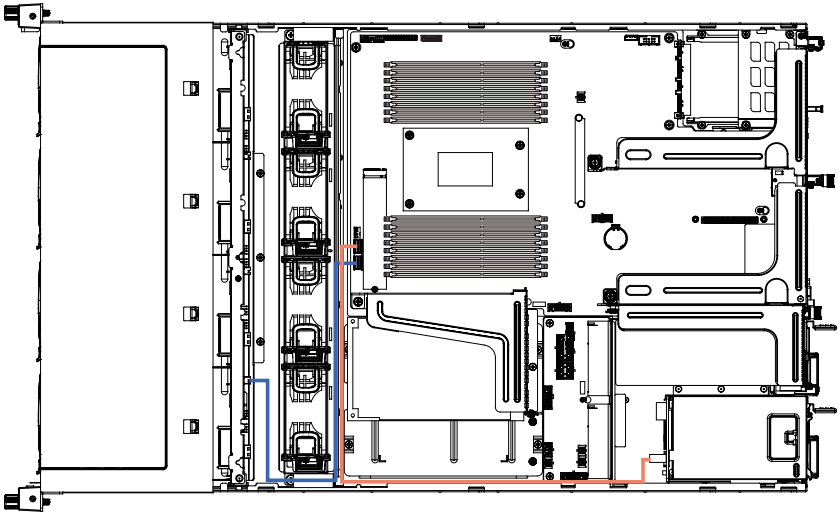
GPU Card#2 Power Cable (for R262-ZA2 only)



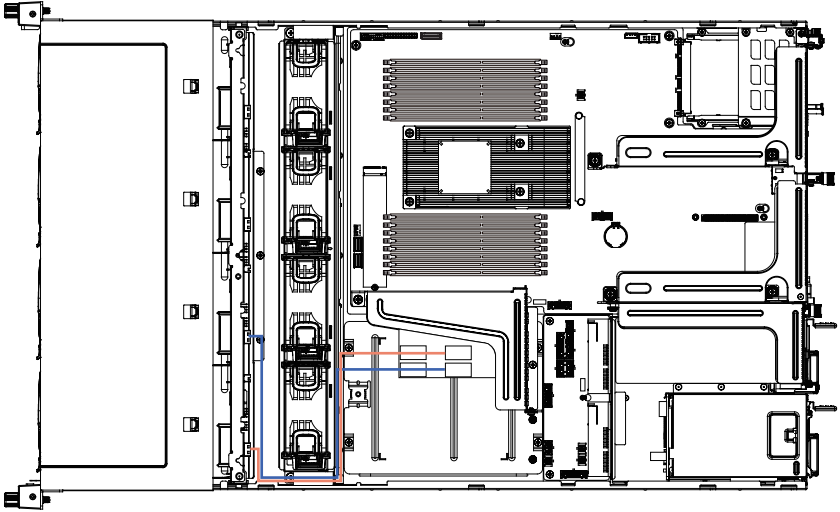
Slimline SAS Cable #0/#1



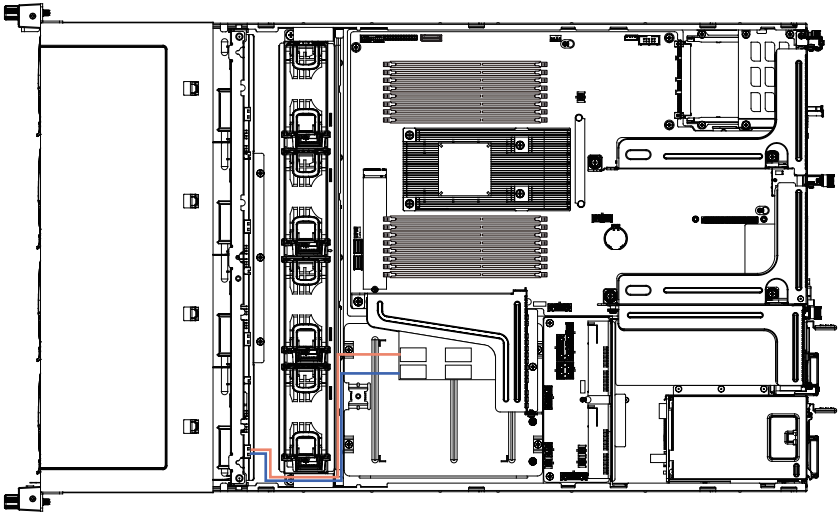
Slimline SAS to SATA Cable #2/#3



Slimline SAS to NVMe Card #0 - #1 (for R262-ZA2 only)

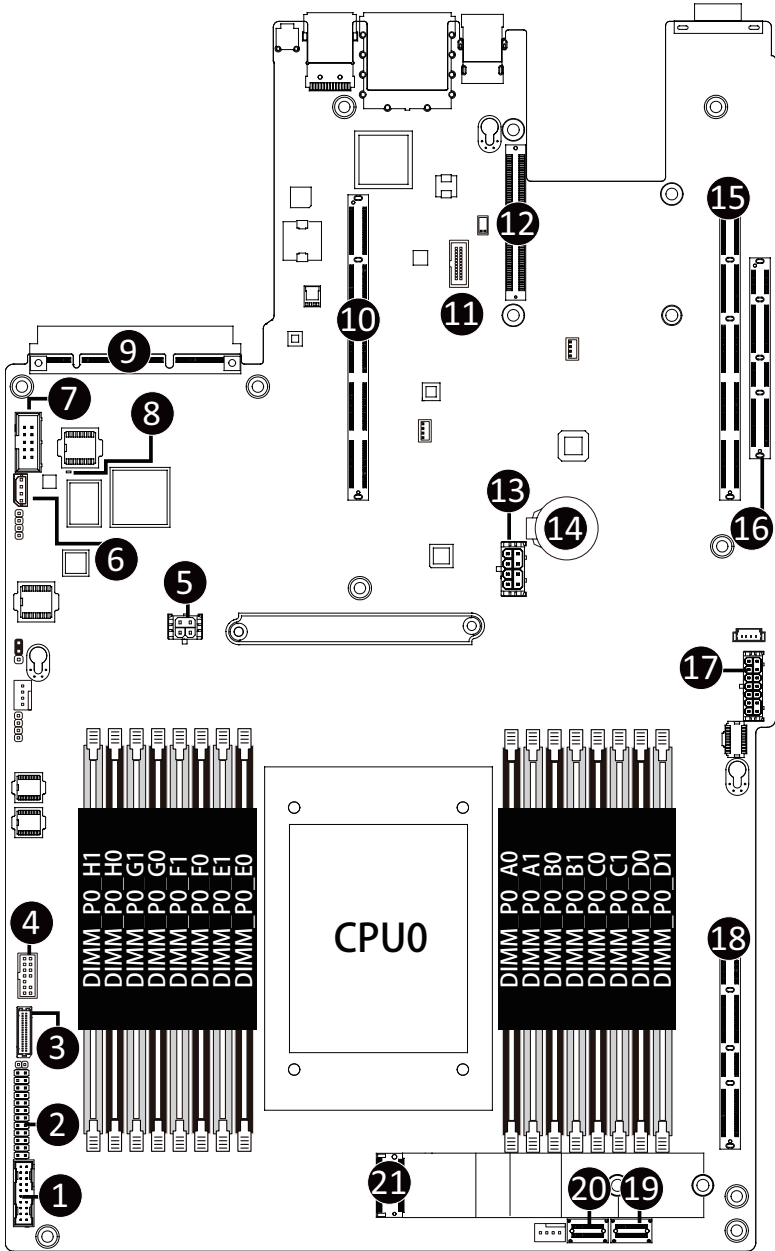


Slimline SAS to NVMe Card #2 - #3 (for R262-ZA2 only)



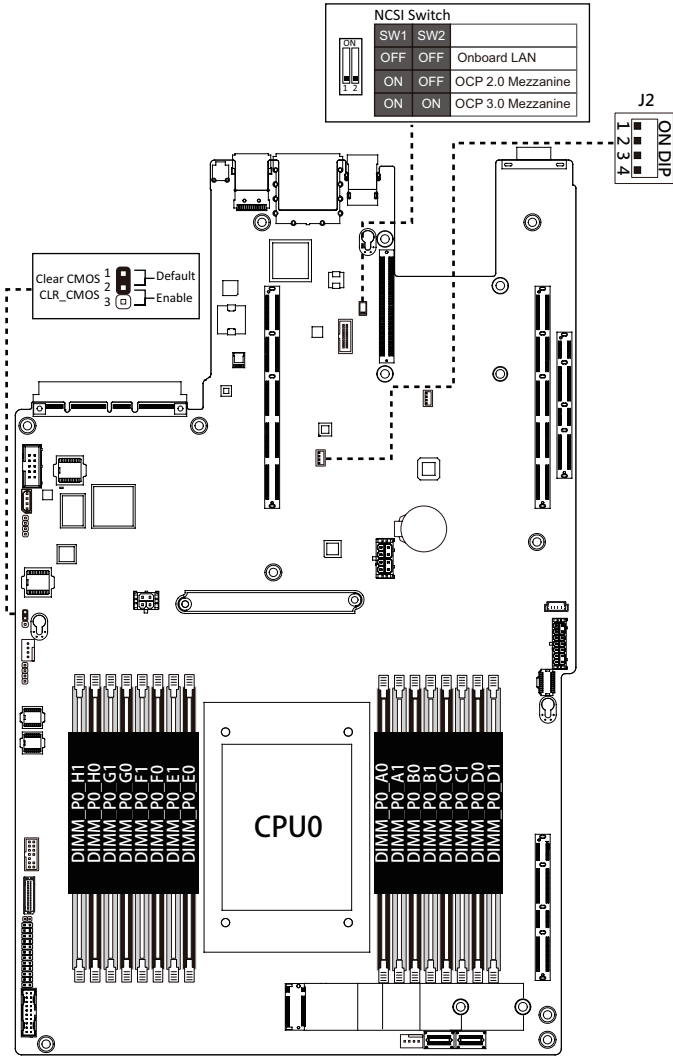
Chapter 4 Motherboard Components

4-1 Motherboard Components



Item	Description
1	Front Panel USB 3.0 Connector
2	Front Panel Connector
3	HDD Back Plane Board Connector
4	TPM Module Connector (SPI Interface)
5	2 x 2 Pin P12V Power Connector
6	IPMB Connector
7	Serial Port Cable Connector
8	BMC Firmware Readiness LED
9	OCP Mezzanine Connector (OCP 3.0/SFF Type/Gen4 x16)
10	Riser Connector #1 (PCIe Gen4/x32 Slot)
11	GbE LAN Cable Connector
12	OCP Mezzanine Connector (OCP 2.0/Gen3 x8)
13	2 x 5 Pin P12V Power Connector
14	System Battery
15	Riser Connector #2 (PCIe Gen4/x32 Slot)
16	Riser Connector #3 (PCIe Gen4/x16 Slot)
17	2 x 6 Pin Power Connector
18	Riser Connector #4 (PCIe Gen4/x16 Slot)
19	SlimLine SAS Connector (SLSAS_0/PCIe/SATA/Defined by SKUs)
20	SlimLine SAS Connector (SLSAS_1/PCIe/SATA/Defined by SKUs)
21	M.2 Connector (PCIe Gen4 x4, Supports NGFF-22110)

4-2 Jumper Setting



J2		ON	OFF
1	HOST_SMBUS_SEL	BIOS defined	
2	PMBUS_SEL	BIOS defined	
3	BIOS_PWD	Clear supervisor password	Normal [Default]
4	BIOS_RCVR	BIOS recovery mode	Normal [Default]

Chapter 5 BIOS Setup

BIOS (Basic Input and Output System) records hardware parameters of the system in the EFI on the motherboard. Its major functions include conducting the Power-On Self-Test (POST) during system startup, saving system parameters, loading the operating system etc. The BIOS includes a BIOS Setup program that allows the user to modify basic system configuration settings or to activate certain system features. When the power is turned off, the battery on the motherboard supplies the necessary power to the CMOS to keep the configuration values in the CMOS.

To access the BIOS Setup program, press the key during the POST when the power is turned on.



- BIOS flashing is potentially risky, if you do not encounter any problems when using the current BIOS version, it is recommended that you don't flash the BIOS. To flash the BIOS, do it with caution. Inadequate BIOS flashing may result in system malfunction.
- It is recommended that you not alter the default settings (unless you need to) to prevent system instability or other unexpected results. Inadequately altering the settings may result in system's failure to boot. If this occurs, try to clear the CMOS values and reset the board to default values. (Refer to the **Exit** section in this chapter or introductions of the battery/clearing CMOS jumper in Chapter 1 for how to clear the CMOS values.)

BIOS Setup Program Function Keys

<<-><->>	Move the selection bar to select the screen
<↑><↓>	Move the selection bar to select an item
<+>	Increase the numeric value or make changes
<->	Decrease the numeric value or make changes
<Enter>	Execute command or enter the submenu
<Esc>	Main Menu: Exit the BIOS Setup program Submenus: Exit current submenu
<F1>	Show descriptions of general help
<F3>	Restore the previous BIOS settings for the current submenus
<F9>	Load the Optimized BIOS default settings for the current submenus
<F10>	Save all the changes and exit the BIOS Setup program

■ **Main**

This setup page includes all the items of the standard compatible BIOS.

■ **Advanced**

This setup page includes all the items of AMI BIOS special enhanced features.

(ex: Auto detect fan and temperature status, automatically configure hard disk parameters.)

■ **AMD CBS**

This setup page includes the common items for configuration of AMD motherboard-related information.

■ **AMD PBS Option**

This setup page includes the common items for configuration of AMD CPM RAS related settings.

■ **Chipset**

This setup page includes all the submenu options for configuring the functions of the North Bridge.

■ **Server Management**

Server additional features enabled/disabled setup menus.

■ **Security**

Change, set, or disable supervisor and user password. Configuration supervisor password allows you to restrict access to the system and BIOS Setup.

A supervisor password allows you to make changes in BIOS Setup.

A user password only allows you to view the BIOS settings but not to make changes.

■ **Boot**

This setup page provides items for configuration of the boot sequence.

■ **Save & Exit**

Save all the changes made in the BIOS Setup program to the CMOS and exit BIOS Setup. (Pressing <F10> can also carry out this task.)

Abandon all changes and the previous settings remain in effect. Pressing <Y> to the confirmation message will exit BIOS Setup. (Pressing <Esc> can also carry out this task.)

5-1 The Main Menu

Once you enter the BIOS Setup program, the Main Menu (as shown below) appears on the screen. Use arrow keys to move among the items and press <Enter> to accept or enter other sub-menu.

Main Menu Help

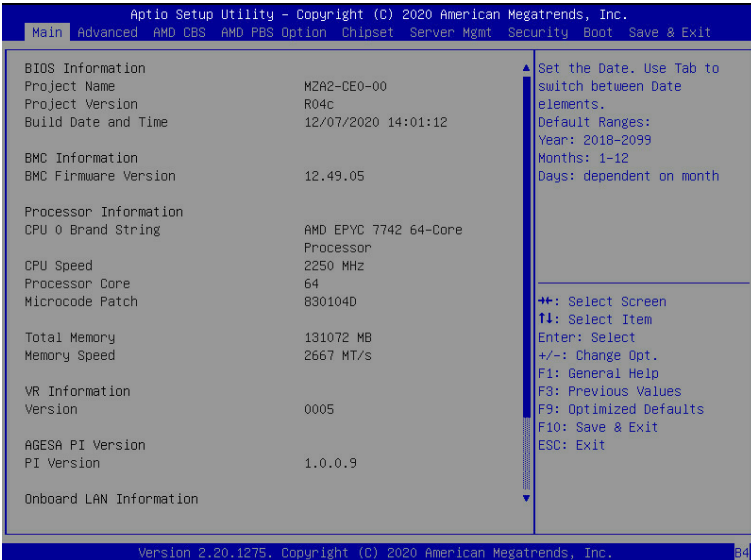
The on-screen description of a highlighted setup option is displayed on the bottom line of the Main Menu.

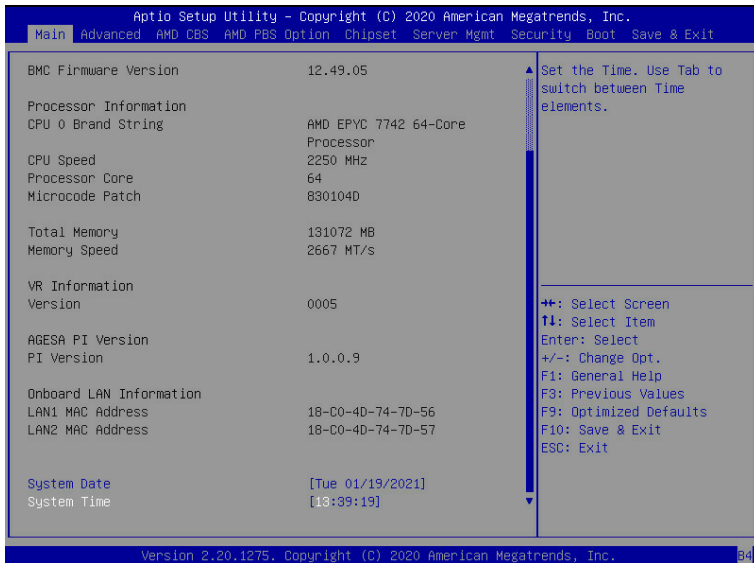
Submenu Help

While in a submenu, press <F1> to display a help screen (General Help) of function keys available for the menu. Press <Esc> to exit the help screen. Help for each item is in the Item Help block on the right side of the submenu.



- When the system is not stable as usual, select the **Restore Defaults** item to set your system to its defaults.
- The BIOS Setup menus described in this chapter are for reference only and may differ by BIOS version.





Parameter	Description
BIOS Information	
Project Name	Displays the project name information.
Project Version	Displays version number of the BIOS setup utility.
Build Date and Time	Displays the date and time when the BIOS setup utility was created.
BMC Information ^(Note1)	
BMC Firmware Version ^(Note1)	Displays BMC firmware version information.
Processor Information	
CPU0 Brand String/ CPU Speed / Processor Core / Microcode Patch	Displays the technical specifications for the installed processor(s).
Memory Information	
Total Memory ^(Note2)	Displays the total memory size of the installed memory.
Memory Speed ^(Note2)	Displays the frequency information of the installed memory.
VR Information Version	Displays VR version information
AGESA PI Version	
PI Version	Displays AGESA PI version information.

(Note1) Functions available on selected models.

(Note2) This section will display capacity and frequency information of the memory that the customer has installed.

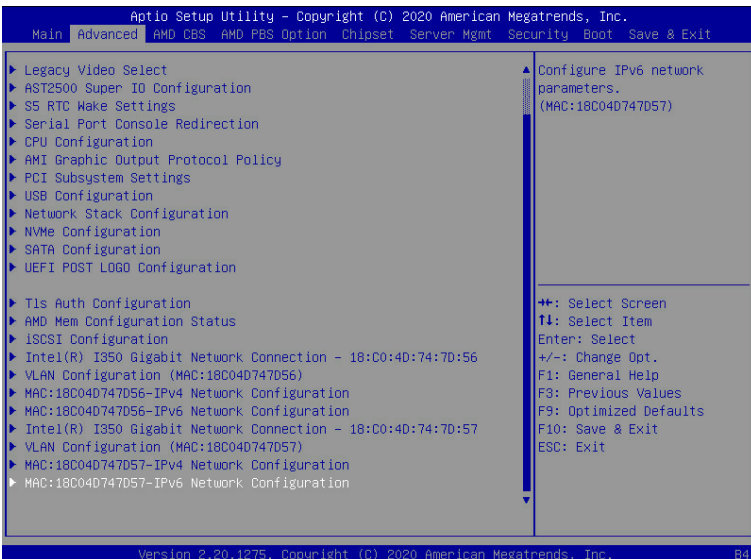
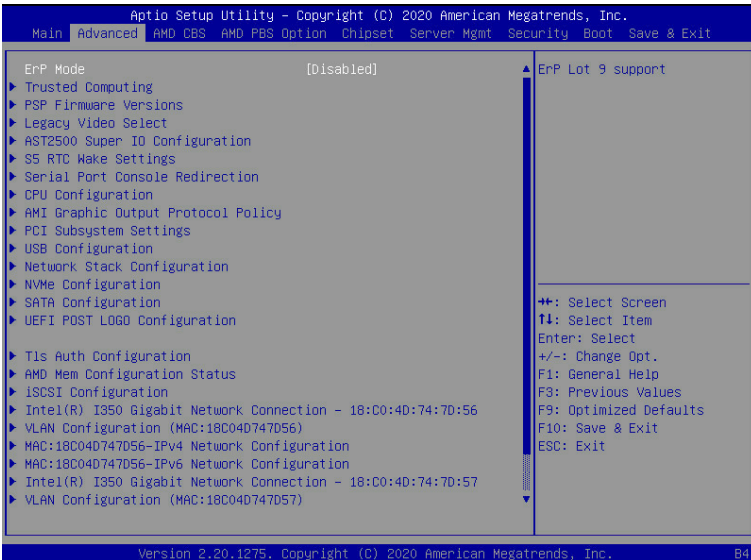
Parameter	Description
Onboard LAN Information	
LAN1 MAC Address ^(Note)	Displays LAN MAC address information.
LAN2 MAC Address ^(Note)	Displays LAN MAC address information.
System Date	Sets the date following the weekday-month-day-year format.
System Time	Sets the system time following the hour-minute-second format.

(Note) The number of LAN ports listed will depend on the motherboard / system model.

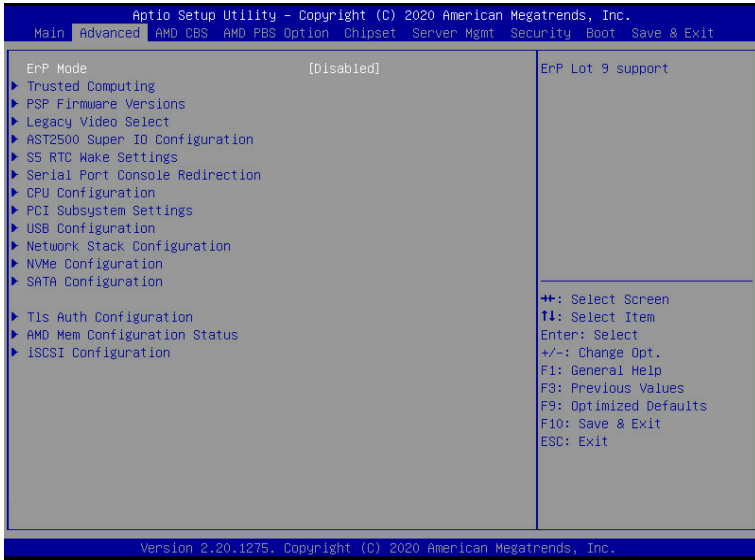
5-2 Advanced Menu

The Advanced Menu displays submenu options for configuring the function of various hardware components. Select a submenu item, then press <Enter> to access the related submenu screen.

When Boot Mode Select is set to UEFI (Default)



When "Boot Mode Select" is set to Legacy in the Boot > Boot Mode Select section



Parameter	Description
ErP Mode (Energy-related Products)	<p>Enable/Disable ErP Lot 9 support. When ErP Mode is enabled, fan speed will be adjusted and any redundant PSU will be placed into a standby state ("Cold Redundancy") in order to decrease power consumption when the server is in idle mode.</p> <p>Options available: Disabled, Lot 9. Default setting is Disabled.</p>

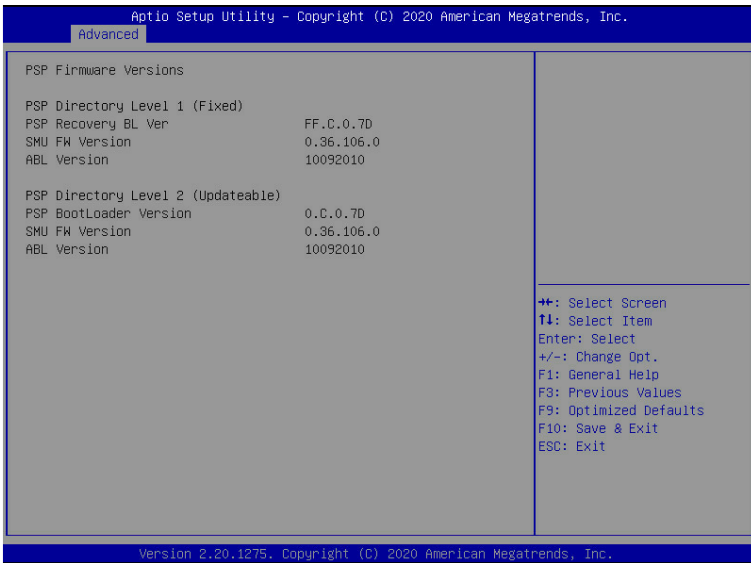
5-2-1 Trusted Computing



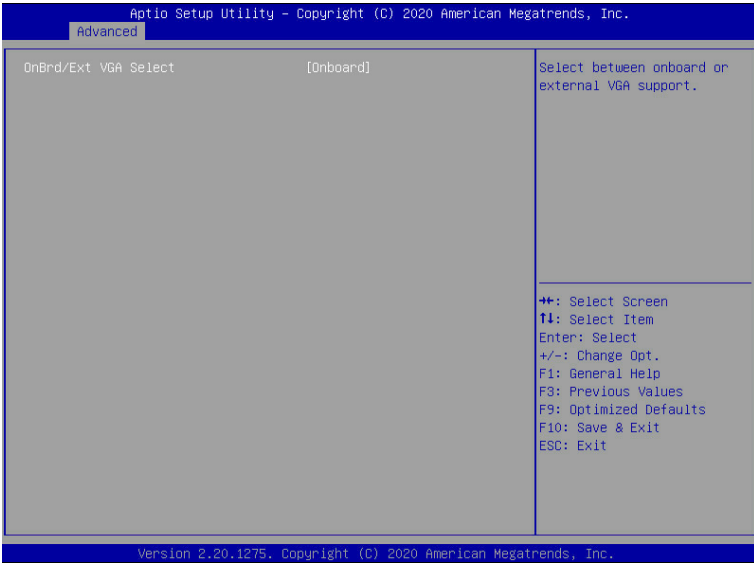
Parameter	Description
Configuration	
Security Device Support	Enable/Disable BIOS support for security device. OS will not show security device. TCG EFI protocol and INT1A interface will not be available. Options available: Enable, Disable. Default setting is Enable .
SPI TPM Support	Select Enable to activate TPM support feature. Options available: Enabled, Disabled. Default setting is Enabled .
Disable Block Sid	Override to allow SID authentication in TCG Storage device. Options available: Enabled, Disabled. Default setting is Disabled .

5-2-2 PSP Firmware Versions

The PSP Firmware Versions page displays the basic PSP firmware version information. Items on this window are non-configurable.



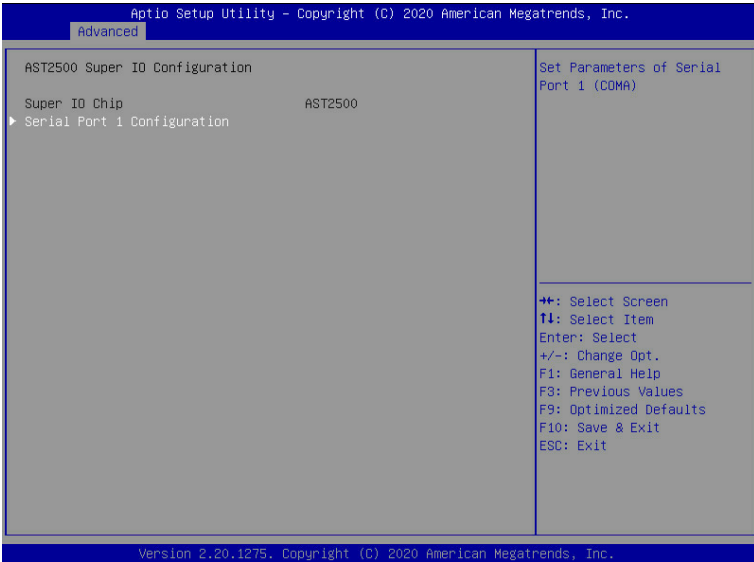
5-2-3 Legacy Video Select



Parameter	Description
OnBrd/Ext VGA Select ^(Note)	Selects between onboard or external VGA support. Options available: Auto, Onboard, External. Default setting is Onboard .

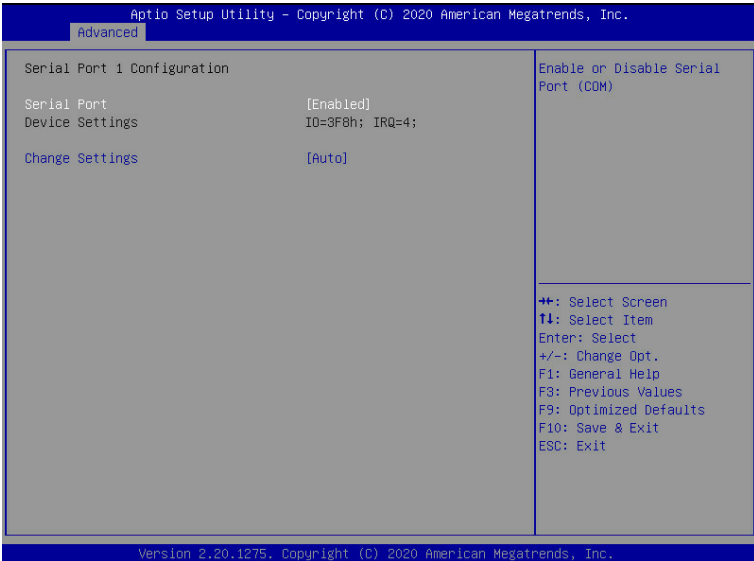
(Note) This configurable option will be displayed when "Boot Mode Select" is set to **Legacy** in the Boot > Boot Mode Select section.

5-2-4 AST2500 Super IO Configuration



Parameter	Description
AST2500 Super IO Configuration	
Super IO Chip	Displays the super IO chip information
Serial Port 1 Configuration	Press [Enter] for configuration of advanced items.

5-2-4-1 Serial Port 1 Configuration

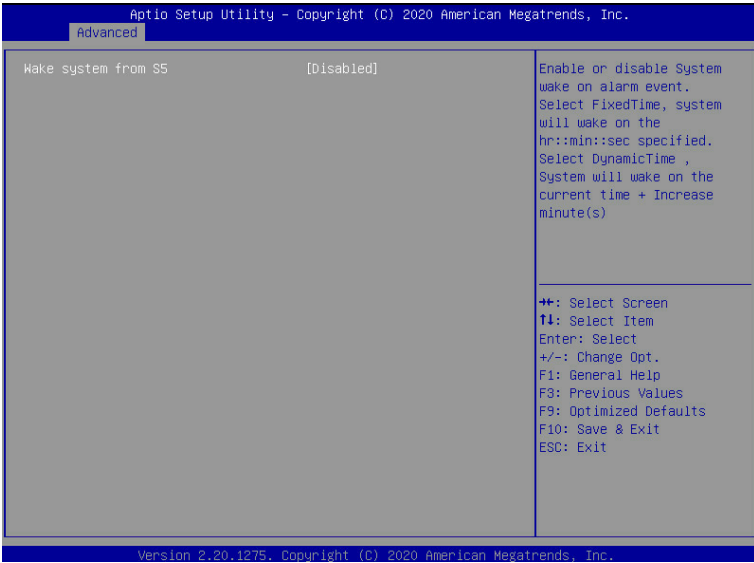


Parameter	Description
Serial Port 1 Configuration	
Serial Port ^(Note1)	Enable/Disable the Serial Port (COM). When set to Enabled allows you to configure the Serial port 1 settings. When set to Disabled, displays no configuration for the serial port. Options available: Enabled, Disabled. Default setting is Enabled .
Devices Settings ^(Note2)	Displays the Serial Port 1 device settings.
Change Settings ^(Note2)	Select an optimal settings for Super IO Device. Options available for Serial Port 1: Auto IO=3F8h; IRQ=4; IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; Default setting is Auto .

(Note1) Advanced items prompt when this item is defined.

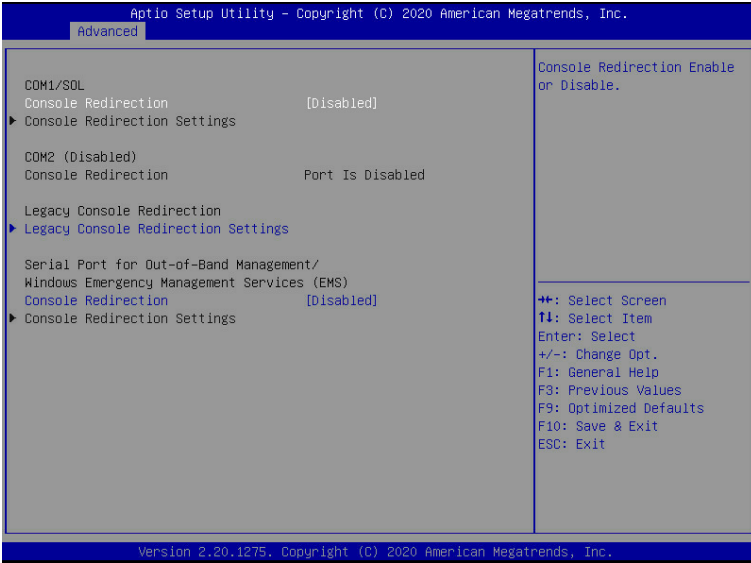
(Note2) This item appears when **Serial Port** is set to **Enabled**.

5-2-5 S5 RTC Wake Settings



Parameter	Description
Wake System from S5	Enable/Disable system wake on alarm event. Options available: Disabled, Fixed Time, Dynamic Time. When Fixed Time is selected, system will wake on the hr::min::sec specified. Default setting is Disabled .

5-2-6 Serial Port Console Redirection



Parameter	Description
COM1/Serial Over LAN Console Redirection ^(Note)	<p>Select whether to enable console redirection for specified device. Console redirection enables the users to manage the system from a remote location.</p> <p>Options available: Enabled, Disabled. Default setting is Disabled.</p>
COM1/Serial Over LAN Console Redirection Settings	<p>Press [Enter] to configure advanced items.</p> <p>Please note that this item is configurable when COM1/Serial Over LAN Console Redirection is set to Enabled.</p> <ul style="list-style-type: none"> ◆ Terminal Type <ul style="list-style-type: none"> – Selects a terminal type to be used for console redirection. – Options available: VT100, VT100+, ANSI, VT-UTF8. Default setting is ANSI. ◆ Bits per second <ul style="list-style-type: none"> – Selects the transfer rate for console redirection. – Options available: 9600, 19200, 38400, 57600, 115200. Default setting is 115200. ◆ Data Bits <ul style="list-style-type: none"> – Selects the number of data bits used for console redirection. – Options available: 7, 8. Default setting is 8.

(Note) Advanced items prompt when this item is defined.

Parameter	Description
COM1/Serial Over LAN Console Redirection Settings (continued)	<ul style="list-style-type: none"> ◆ Parity <ul style="list-style-type: none"> – A parity bit can be sent with the data bits to detect some transmission errors. – Even: parity bit is 0 if the num of 1's in the data bits is even. – Odd: parity bit is 0 if num of 1's in the data bits is odd. – Mark: parity bit is always 1. Space: Parity bit is always 0. – Mark and Space Parity do not allow for error detection. – Options available: None, Even, Odd, Mark, Space. Default setting is None. ◆ Stop Bits <ul style="list-style-type: none"> – Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. – Options available: 1, 2. Default setting is 1. ◆ Flow Control <ul style="list-style-type: none"> – Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals. – Options available: None, Hardware RTS/CTS. Default setting is None. ◆ VT-UTF8 Combo Key Support <ul style="list-style-type: none"> – Enable/Disable the VT-UTF8 Combo Key Support. – Options available: Enabled, Disabled. Default setting is Enabled. ◆ Recorder Mode^(Note) <ul style="list-style-type: none"> – When this mode enabled, only texts will be send. This is to capture Terminal data. – Options available: Enabled, Disabled. Default setting is Disabled. ◆ Resolution 100x31^(Note) <ul style="list-style-type: none"> – Enable/Disable extended terminal resolution. – Options available: Enabled, Disabled. Default setting is Enabled. ◆ Putty KeyPad^(Note) <ul style="list-style-type: none"> – Selects FunctionKey and KeyPad on Putty. – Options available: VT100, LINUX, XTERMR6, SC0, ESCN, VT400. Default setting is VT100.

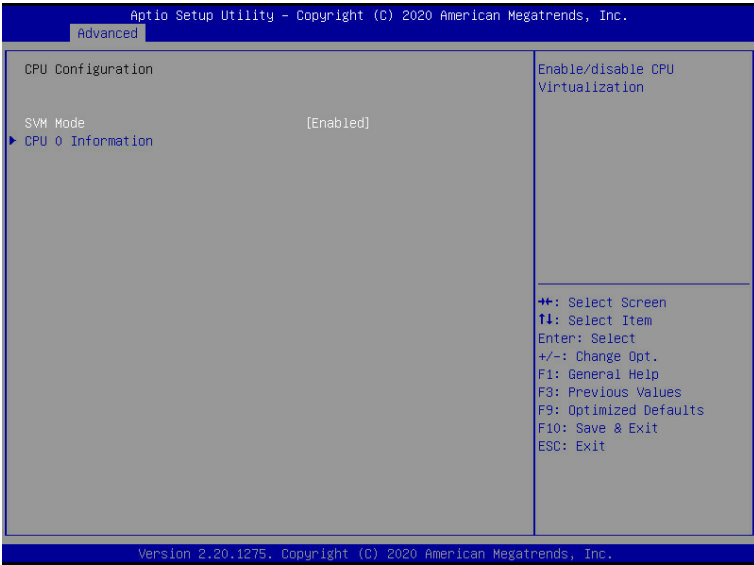
(Note) Advanced items prompt when this item is defined.

Parameter	Description
Legacy Console Redirection	
Legacy Console Redirection Settings	<p>Press [Enter] to configure advanced items.</p> <ul style="list-style-type: none"> ◆ Redirection COM Port <ul style="list-style-type: none"> – Selects a COM port for Legacy serial redirection. – Default setting is COM1/SOL. ◆ Resolution <ul style="list-style-type: none"> – Selects the number of rows and columns used in Console Redirection for legacy OS support. – Options available: 80x24, 80x25. Default setting is 80x24. ◆ Redirect After POST <ul style="list-style-type: none"> – When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. – Options available: Always Enable, BootLoader. Default setting is Always Enable.
Serial Port for Out-of-Band Management / Windows Emergency Management Services (EMS) Console Redirection ^(Note)	<p>EMS console redirection allows the user to configure Console Redirection Settings to support Out-of-Band Serial Port management.</p> <p>Options available: Enabled, Disabled. Default setting is Disabled.</p>
Serial Port for Out-of-Band EMS Console Redirection Settings	<p>Press [Enter] to configure advanced items.</p> <p>Please note that this item is configurable when Serial Port for Out-of-Band Management EMS Console Redirection is set to Enabled.</p> <ul style="list-style-type: none"> ◆ Out-of-Band Mgmt Port <ul style="list-style-type: none"> – Microsoft Windows Emergency Management Service (EMS) allows for remote management of a Windows Server OS through a serial port. – Default setting is COM1/SOL. ◆ Terminal Type <ul style="list-style-type: none"> – Selects a terminal type to be used for console redirection. – Options available: VT100, VT100+, ANSI, VT-UTF8. Default setting is ANSI. ◆ Bits per second <ul style="list-style-type: none"> – Selects the transfer rate for console redirection. – Options available: 9600, 19200, 38400, 57600, 115200. Default setting is 115200.

(Note) Advanced items prompt when this item is defined.

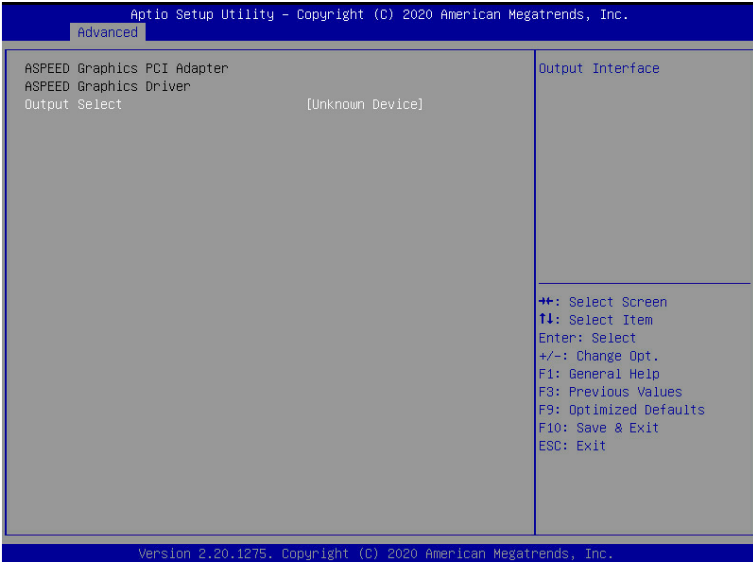
Parameter	Description
Serial Port for Out-of-Band EMS Console Redirection Settings(continued)	<ul style="list-style-type: none">◆ Flow Control<ul style="list-style-type: none">– Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.– Options available: None, Hardware RTS/CTS, Software Xon/Xoff. Default setting is None.

5-2-7 CPU Configuration



Parameter	Description
CPU Configuration	
SVM Mode	Enable/Disable the CPU Virtualization. Options available: Enabled, Disabled. Default setting is Enabled .
CPU 0 Information	Press [Enter] to view the memory information related to CPU 0.

5-2-8 AMI Graphic Output Protocol Policy



Parameter	Description
ASPEED Graphics PCI Adapter	
ASPEED Graphics Driver	
Output Select	Selects Monitor Output by Graphic Output Protocol.

5-2-9 PCI Subsystem Settings

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Advanced

PCI Bus Driver Version	A5.01.19	▲ Change SLOT1_FRONT 1 PCIe Lanes. ++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F3: Previous Values F9: Optimized Defaults F10: Save & Exit ESC: Exit
SLOT1_FRONT Lanes	[Auto]	
SLOT1_FRONT I/O ROM	[Enabled]	
SLOT1_FRONT Max Link Speed	[Auto]	
SLOT1_REAR Lanes	[Auto]	
SLOT1_REAR ROM	[Enabled]	
SLOT1_REAR Max Link Speed	[Auto]	
SLOT2_FRONT Lanes	[Auto]	
SLOT2_FRONT I/O ROM	[Enabled]	
SLOT2_FRONT Max Link Speed	[Auto]	
SLOT2_REAR Lanes	[Auto]	
SLOT2_REAR I/O ROM	[Enabled]	
SLOT2_REAR Max Link Speed	[Auto]	
SLOT3 Lanes	[Auto]	
SLOT3 I/O ROM	[Enabled]	
SLOT3 Max Link Speed	[Auto]	
OCP1 Lanes	[Auto]	
OCP1 I/O ROM	[Enabled]	
OCP1 Max Link Speed	[Auto]	

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Advanced

SLOT2_REAR Max Link Speed	[Auto]	▲ If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support. ++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F3: Previous Values F9: Optimized Defaults F10: Save & Exit ESC: Exit
SLOT3 Lanes	[Auto]	
SLOT3 I/O ROM	[Enabled]	
SLOT3 Max Link Speed	[Auto]	
OCP1 Lanes	[Auto]	
OCP1 I/O ROM	[Enabled]	
OCP1 Max Link Speed	[Auto]	
OCP2 Lanes	[Auto]	
OCP2 I/O ROM	[Enabled]	
OCP2 Max Link Speed	[Auto]	
SLOT4 Lanes	[Auto]	
SLOT4 I/O ROM	[Enabled]	
SLOT4 Max Link Speed	[Auto]	
Onboard LAN Controller	[Enabled]	
Onboard LAN1 I/O ROM	[Enabled]	
Onboard LAN2 I/O ROM	[Enabled]	
PCI Devices Common Settings:		
Above 4G Decoding	[Enabled]	
SR-IOV Support	[Enabled]	

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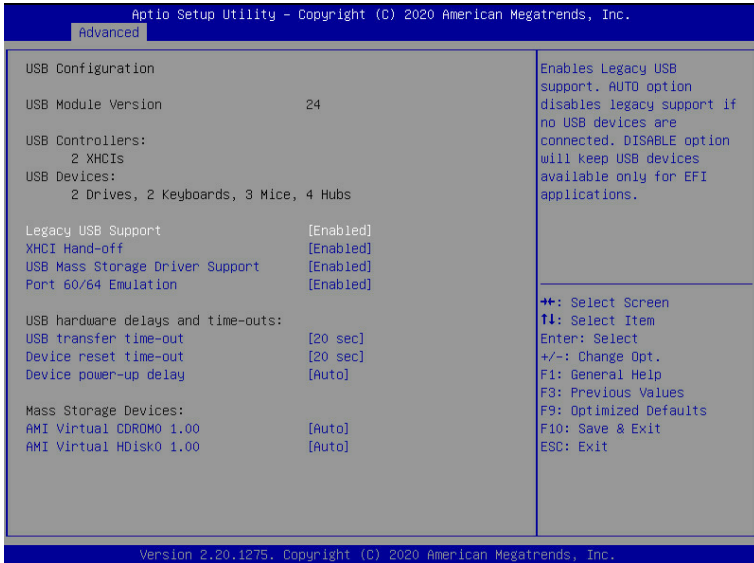
Parameter	Description
PCI Bus Driver Version	Displays the PCI Bus Driver version information.
SLOT_# Lanes Configuration ^(Note1)	Change the PCIe lanes. Options available: Disabled, Auto, x16, x8x8, x8x4x4, x4x4x8, x4x4x4x4. Default setting is Auto .
SLOT Slot # I/O ROM ^(Note1)	When enabled, this setting will initialize the device expansion ROM for the related PCI-E slot. Options available: Enabled, Disabled. Default setting is Enabled .
SLOT Slot # Max Link ^(Note1)	Configure PCIe max link speed. Options available: Auto, Maximum, Gen1, Gen2, Gen3, Gen4. Default setting is Auto .
OCP# Lanes ^(Note2)	Change mezzanine PCIe lanes. Options available: Auto, x16, x8x8, x8x4x4, x4x4x8, x4x4x4x4, Disabled. Default setting is Auto .
OCP# I/O ROM ^(Note2)	When enabled, this setting will initialize the device expansion ROM for the related U.2 device. Options available: Enabled, Disabled. Default setting is Enabled .
OCP# Max Link Speed ^(Note2)	Configure mezzanine OCP max link speed. Options available: Auto, Maximum, Gen1, Gen2, Gen3, Gen4. Default setting is Auto .
Onboard LAN Controller ^(Note3)	Enable/Disable the onboard LAN controller. Options available: Enabled, Disabled. Default setting is Enabled .
Onboard LAN1/2 I/O ROM ^(Note3)	Enable/Disable the onboard LAN devices, and initializes device expansion ROM. Options available: Enabled, Disabled. Default setting is Enabled .
PCI Devices Common Settings	
Above 4G Decoding	Enable/Disable memory mapped I/O to 4GB or greater address space (Above 4G Decoding). Options available: Enabled, Disabled. Default setting is Enabled .
SR-IOV Support	If the system has SR-IOV capable PCIe devices, this item Enable/Disable Single Root IO Virtualization Support. Options available: Enabled, Disabled. Default setting is Disabled .

(Note1) This section is dependent on the available PCIe Slot.

(Note2) This section is dependent on the available OCP connector.

(Note3) This section is dependent on the available LAN controller.

5-2-10 USB Configuration

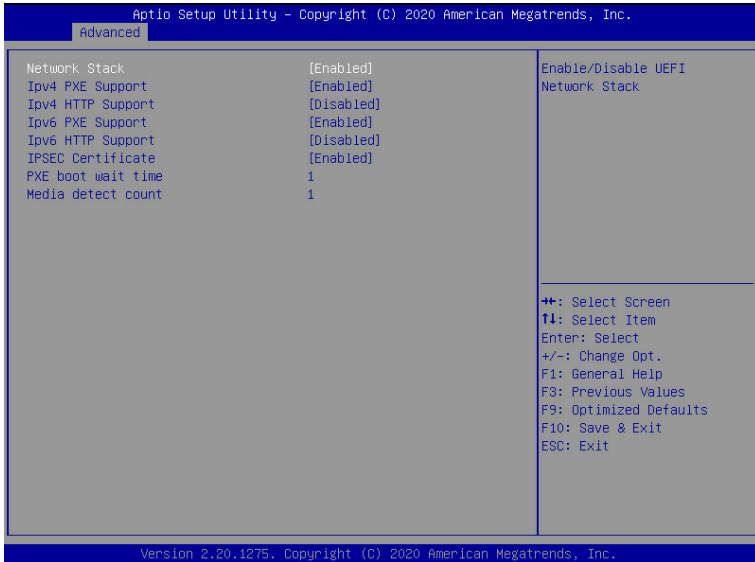


Parameter	Description
USB Configuration	
USB Module Version	Displays the USB module version information.
USB Controllers	Displays the supported USB controllers.
USB Devices	Displays the USB devices connected to the system.
Legacy USB Support	Enable/Disable the Legacy USB support function. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications. Options available: Auto, Enabled, Disabled. Default setting is Enabled .
XHCI Hand-off	Enable/Disable the XHCI Hand-off support. Options available: Enabled, Disabled. Default setting is Enabled .
USB Mass Storage Driver Support ^(Note)	Enable/Disable the USB Mass Storage Driver Support. Options available: Enabled, Disabled. Default setting is Enabled .
Port 60/64 Emulation	Enables the I/O port 60h/64h emulation support. This should be enabled for the complete USB Keyboard Legacy support for non-USB aware OS. Options available: Enabled, Disabled. Default setting is Enabled .

(Note) This item is present only if you attach USB devices.

Parameter	Description
USB hardware delays and time-outs	
USB transfer time-out	Selects the time-out value for USB Control/Bulk/Interrupt transfers. Options available: 1 sec, 5 sec, 10 sec, 20 sec. Default setting is 20 sec .
Device reset time-out	Selects the time-out value during a USB mass storage device reset. Options available: 10 sec, 20 sec, 30 sec, 40 sec. Default setting is 20 sec .
Device power-up delay	Maximum time the device will take before it properly reports itself to the Host Controller. "Auto" uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor. Options available: Auto, Manual. Default setting is Auto .
Mass Storage Devices	Displays the mass storage devices available on the system.

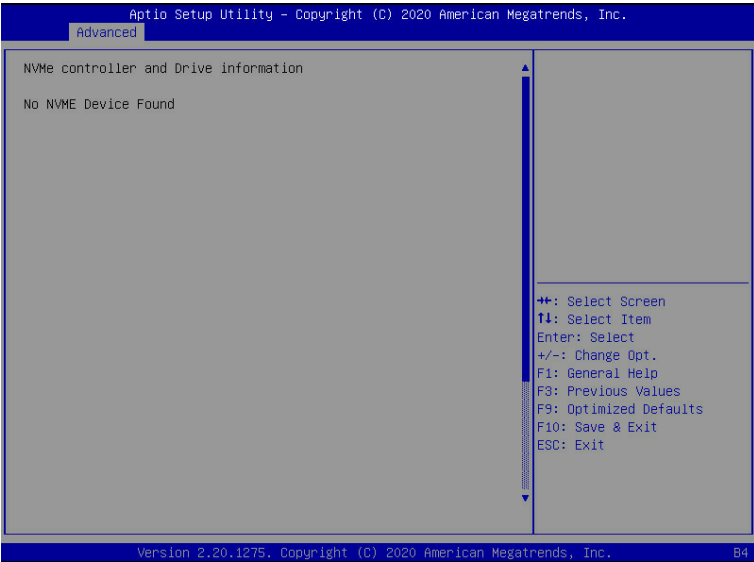
5-2-11 Network Stack Configuration



Parameter	Description
Network Stack	Enable/Disable the UEFI network stack. Options available: Enabled, Disabled. Default setting is Enabled .
Ipv4 PXE Support ^(Note)	Enable/Disable the Ipv4 PXE feature. Options available: Enabled, Disabled. Default setting is Enabled .
Ipv4 HTTP Support ^(Note)	Enable/Disable the Ipv4 HTTP feature. Options available: Enabled, Disabled. Default setting is Disabled .
Ipv6 PXE Support ^(Note)	Enable/Disable the Ipv6 PXE feature. Options available: Enabled, Disabled. Default setting is Enabled .
Ipv6 HTTP Support ^(Note)	Enable/Disable the Ipv6 HTTP feature. Options available: Enabled, Disabled. Default setting is Disabled .
IPSEC Certificate ^(Note)	Enable/Disable the IPSEC Certificate feature. Options available: Enabled, Disabled. Default setting is Enabled .
PXE boot wait time ^(Note)	Wait time in seconds to press ESC key to abort the PXE boot. Press the <+> / <-> keys to increase or decrease the desired values.
Media detect count ^(Note)	Number of times the presence of media will be checked. Press the <+> / <-> keys to increase or decrease the desired values.

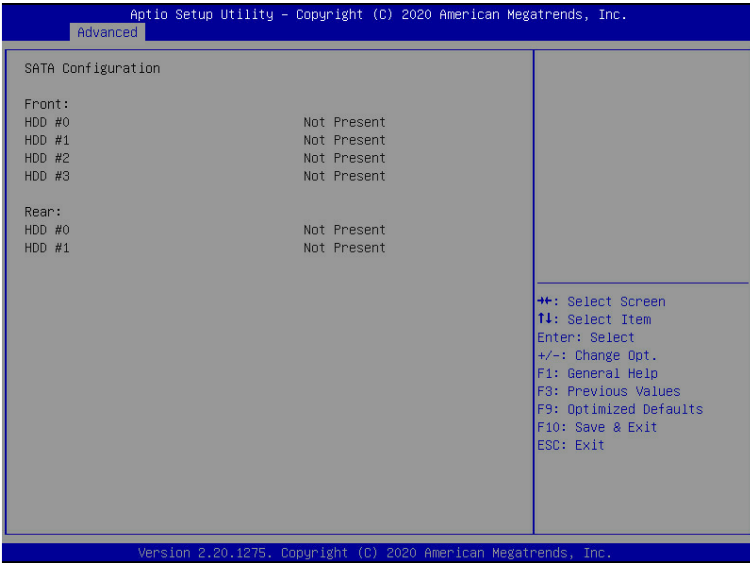
(Note) This item appears when **Network Stack** is set to **Enabled**.

5-2-12 NVMe Configuration



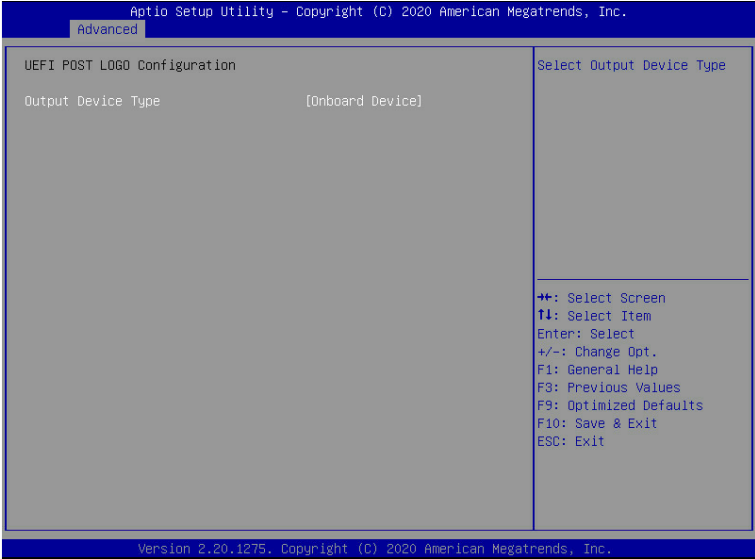
Parameter	Description
NVMe Configuration	Displays the NVMe devices connected to the system.

5-2-13 SATA Configuration



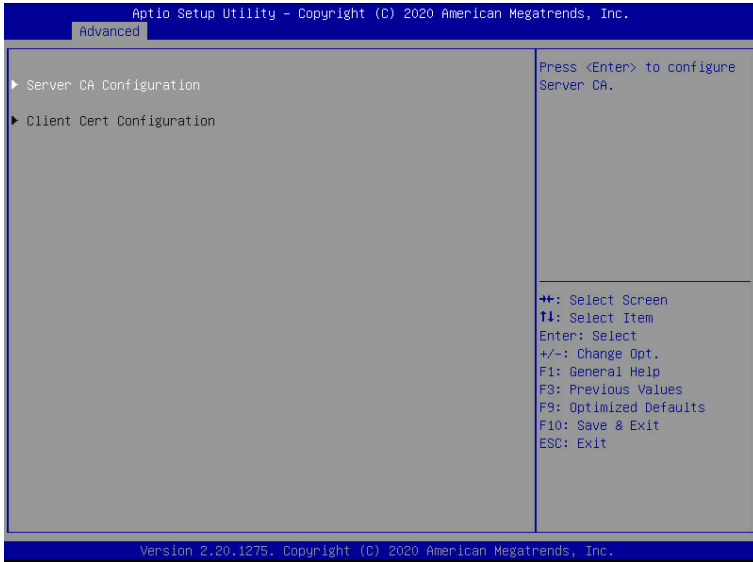
Parameter	Description
SATA Configuration	Displays the installed HDD devices information. System will automatically detect HDD type.

5-2-14 UEFI POST LOGO Configuration



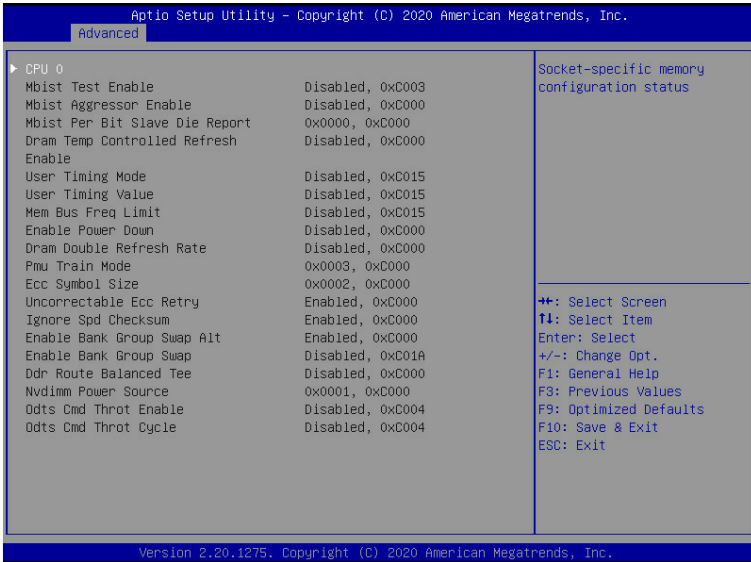
Parameter	Description
Output Device Type	Selects output device type. Options available: First loaded Device, Onboard Device, External Device, Specific Device. Default setting is Onboard Device .

5-2-15 T1s Auth Configuration



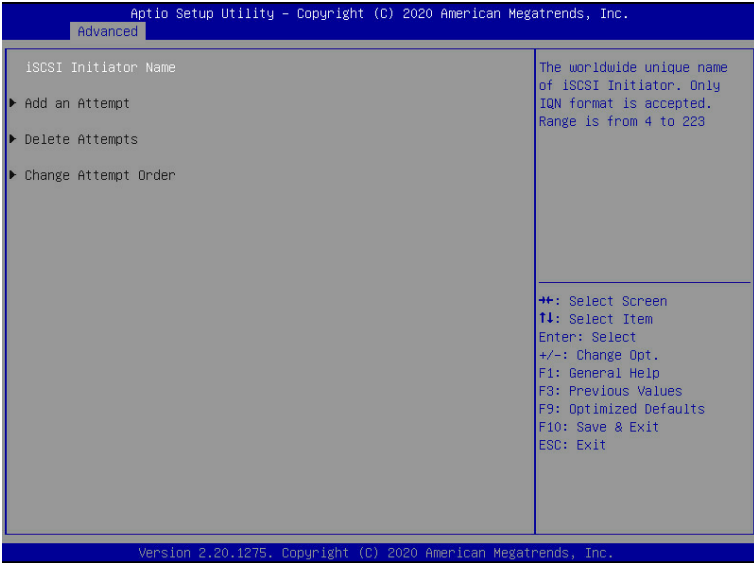
Parameter	Description
Server CA Configuration	Press [Enter] for configuration of advanced items. <ul style="list-style-type: none"> ◆ Enroll Cert <ul style="list-style-type: none"> – Press [Enter] to enroll a certificate <ul style="list-style-type: none"> • Enroll Cert Using File • Cert GUID <ul style="list-style-type: none"> Input digit character in 1111111-2222-3333-4444-1234567890ab format. – Commit Changes and Exit – Discard Changes and Exit ◆ Delete Cert
Client Cert Configuration	Press [Enter] for configuration of advanced items.

5-2-16 AMD Mem Configuration Status



Parameter	Description
CPU0	Press [Enter] to view the memory configuration status related to CPU 0.

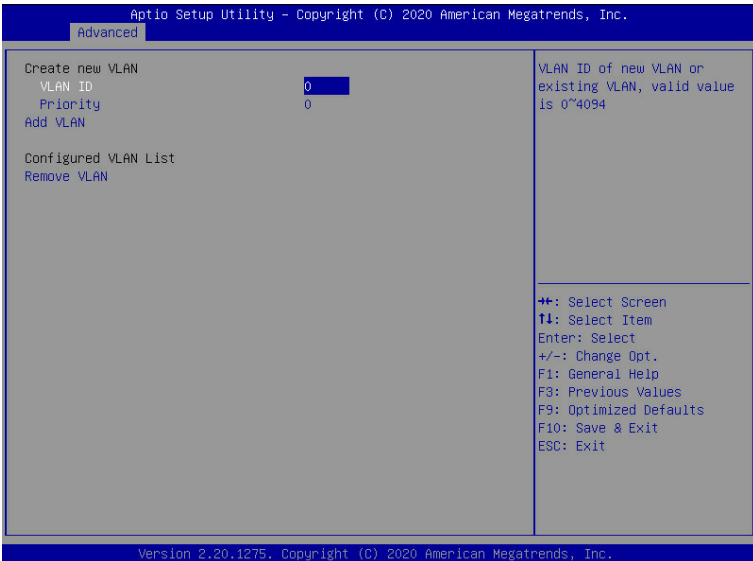
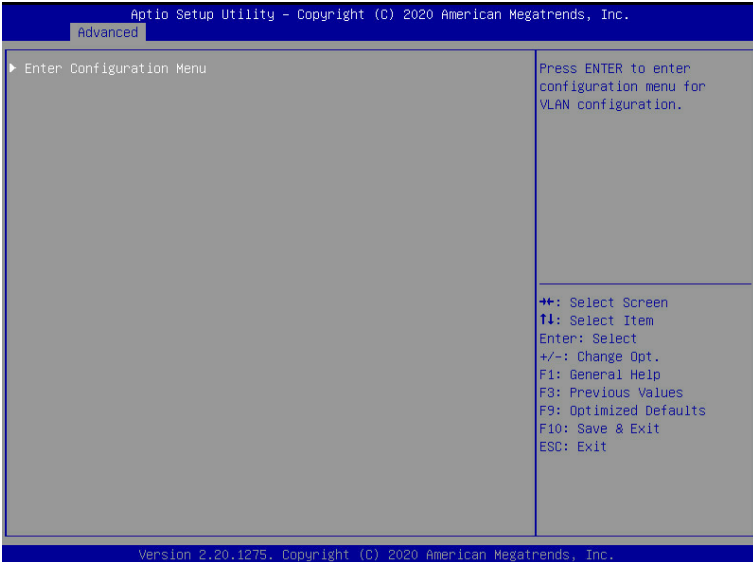
5-2-17 iSCSI Configuration



Parameter	Description
iSCSI Initiator Name	Press [Enter] and name iSCSI Initiator. Only IQN format is accepted. Range: from 4 to 223
Add an Attempt	Press [Enter] to configure advanced items.
Delete Attempts	Press [Enter] to configure advanced items.
Change Attempt Order	Press [Enter] to configure advanced items.

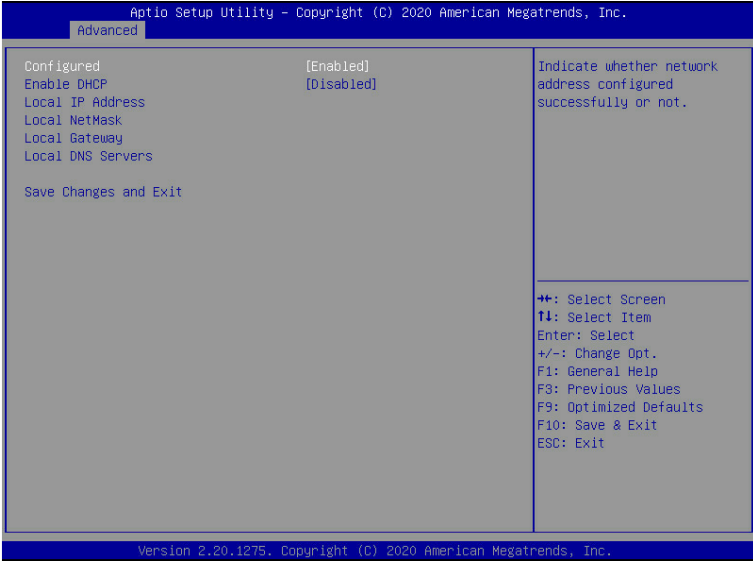
Parameter	Description
NIC Configuration	<ul style="list-style-type: none"> ◆ Link Speed <ul style="list-style-type: none"> – Allows for automatic link speed adjustment. – Options available: Auto Negotiated, 10 Mbps Half, 10 Mbps Full, 100 Mbps Half, 100 Mbps Full. Default setting is Auto Negotiated. ◆ Wake On LAN <ul style="list-style-type: none"> – Enables power on of the system via LAN. Note that configuring Wake on LAN in the operating system does not change the value of this setting, but does override the behavior of Wake on LAN in OS controlled power states. – Options available: Enabled/Disabled. Default setting is Enabled.
Blink LEDs	Identifies the physical network port by blinking the associated LED. Press the numeric keys to adjust desired values.
UEFI Driver	Displays the technical specifications for the Network Interface Controller.
Adapter PBA	Displays the technical specifications for the Network Interface Controller.
Device Name	Displays the technical specifications for the Network Interface Controller.
Chip Type	Displays the technical specifications for the Network Interface Controller.
PCI Device ID	Displays the technical specifications for the Network Interface Controller.
PCI Address	Displays the technical specifications for the Network Interface Controller.
Link Status	Specifies the link status of the port.
MAC Address	Displays the MAC address of the Ethernet controller.
Virtual MAC Address	Displays the virtual MAC address of the Ethernet controller.

5-2-19 VLAN Configuration



Parameter	Description
Enter Configuration Menu	<p data-bbox="338 158 674 181">Press [Enter] to configure advanced items.</p> <ul style="list-style-type: none"> <li data-bbox="338 189 520 213">◆ Create new VLAN <li data-bbox="338 221 447 244">◆ VLAN ID <ul style="list-style-type: none"> <li data-bbox="376 247 804 271">– Sets VLAN ID for a new VLAN or an existing VLAN. <li data-bbox="376 275 937 299">– Press the <+> / <-> keys to increase or decrease the desired values. <li data-bbox="376 304 663 327">– The valid range is from 0 to 4094. <li data-bbox="338 335 434 359">◆ Priority <ul style="list-style-type: none"> <li data-bbox="376 362 852 385">– Sets 802.1Q Priority for a new VLAN or an existing VLAN. <li data-bbox="376 390 937 413">– Press the <+> / <-> keys to increase or decrease the desired values. <li data-bbox="376 418 634 442">– The valid range is from 0 to 7. <li data-bbox="338 450 461 473">◆ Add VLAN <ul style="list-style-type: none"> <li data-bbox="376 476 905 500">– Press [Enter] to create a new VLAN or update an existing VLAN. <li data-bbox="338 508 551 531">◆ Configured VLAN List <li data-bbox="338 539 495 562">◆ Remove VLAN <ul style="list-style-type: none"> <li data-bbox="376 566 732 589">– Press [Enter] to remove an existing VLAN.

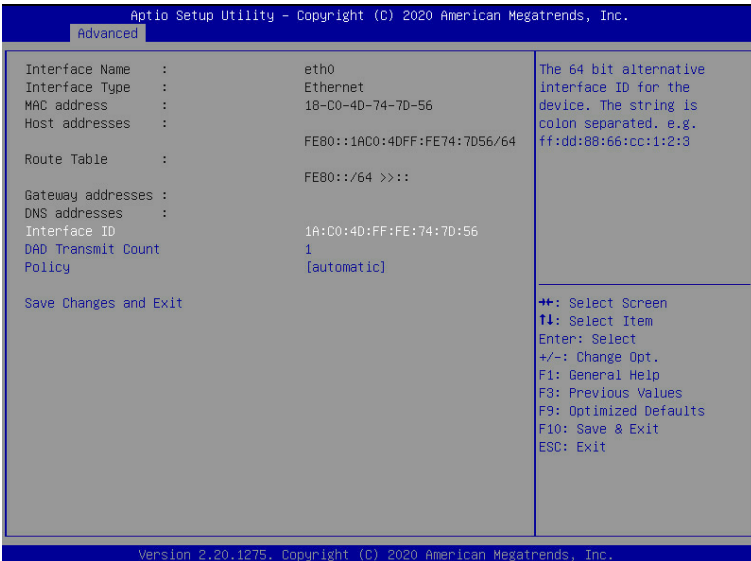
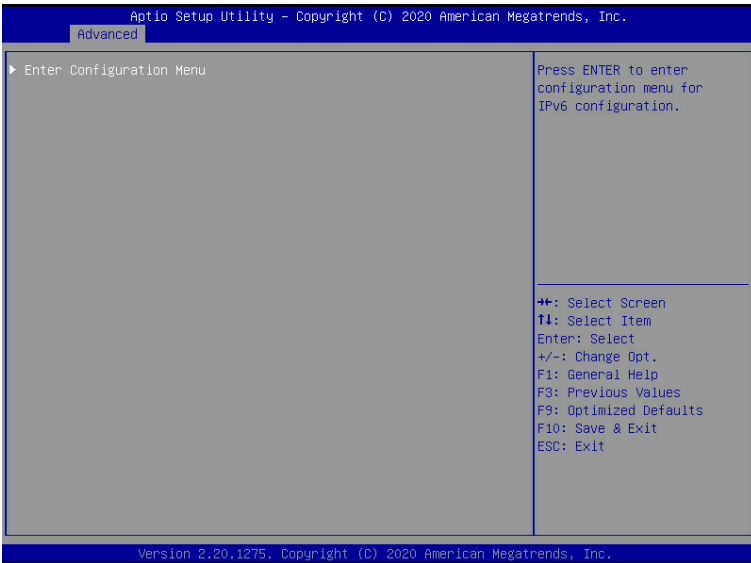
5-2-20 MAC IPv4 Network Configuration



Parameter	Description
Configured	Indicates whether network address is configured successfully or not. Options available: Enabled, Disabled. Default setting is Disabled .
Enable DHCP ^(Note)	Options available: Enabled, Disabled. Default setting is Disabled .
Local IP Address ^(Note)	Press [Enter] to configure local IP address.
Local NetMask ^(Note)	Press [Enter] to configure local NetMask.
Local Gateway ^(Note)	Press [Enter] to configure local Gateway
Local DNS Servers ^(Note)	Press [Enter] to configure local DNS servers
Save Changes and Exit	Press [Enter] to save all configurations.

(Note) This item appears when **Configured** is set to **Enabled**.

5-2-21 MAC IPv6 Network Configuration



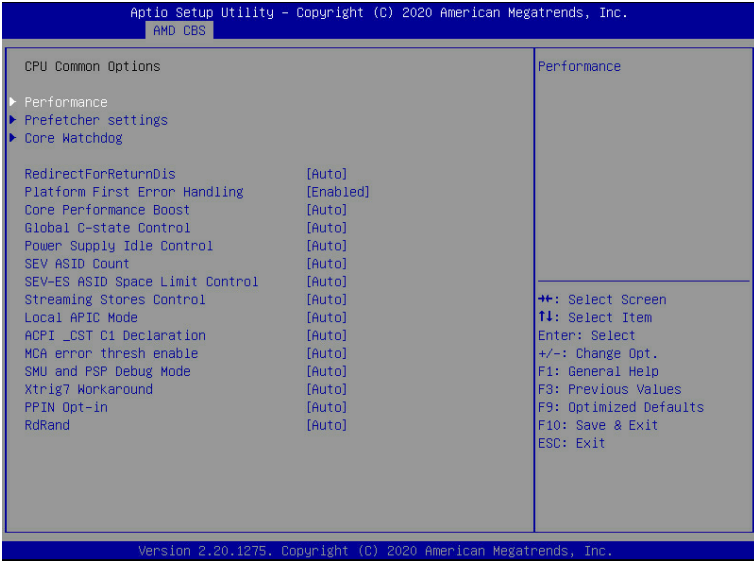
Parameter	Description
Enter Configuration Menu	<p data-bbox="338 158 674 181">Press [Enter] to configure advanced items.</p> <ul style="list-style-type: none"> <li data-bbox="338 189 685 213">◆ Displays the MAC Address information. <li data-bbox="338 221 942 299">◆ Interface ID <ul style="list-style-type: none"> <li data-bbox="376 244 942 299">– The 64 bit alternative interface ID for the device. The string is colon separated. e.g. ff:dd:88:66:cc:1:2:3. <li data-bbox="338 307 942 448">◆ DAD Transmit Count <ul style="list-style-type: none"> <li data-bbox="376 330 942 448">– The number of consecutive Neighbor solicitation messages sent while performing Duplicate Address Detection on a tentative address. A value of zero indicates that Duplicate Address Detection is not performed. <li data-bbox="338 456 942 511">◆ Policy <ul style="list-style-type: none"> <li data-bbox="376 479 942 511">– Options available: automatic, manual. Default setting is automatic. <li data-bbox="338 519 708 562">◆ Save Changes and Exit <ul style="list-style-type: none"> <li data-bbox="376 542 708 562">– Press [Enter] to save all configurations.

5-3 AMD CBS Menu

AMD CBS menu displays submenu options for configuring the CPU-related information that the BIOS automatically sets. Select a submenu item, then press [Enter] to access the related submenu screen.



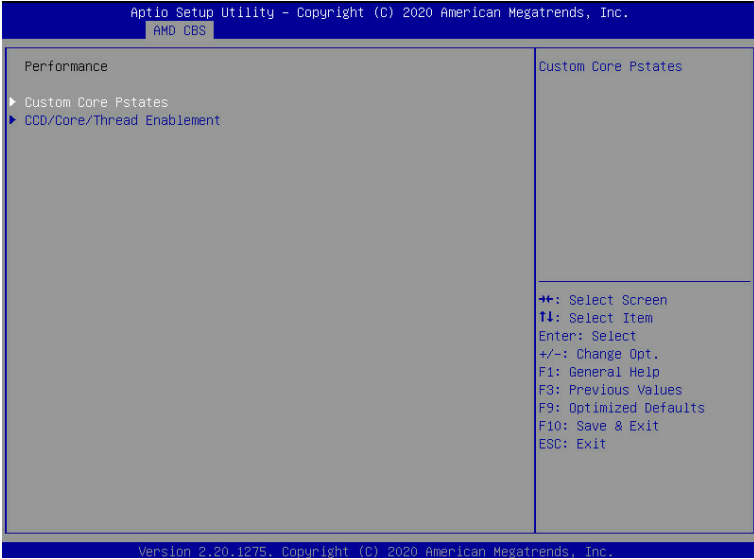
5-3-1 CPU Common Options



Parameter	Description
CPU Common Options	
Performance	Press [Enter] for configuration of advanced items.
Prefetcher settings	Press [Enter] for configuration of advanced items.
Core Watchdog	Press [Enter] for configuration of advanced items.
RedirectForReturnDis	From a workaround for GCC/C000005 issue for XV Core on CZ A0, setting MSRC001_1029 Decode Configuration (DE_CFG) bit 14 [DecfgNoRdrcForReturns] to 1. Options available: Auto, 1, 0. Default setting is Auto .
Platform First Error Handling	Enable/Disable PFEH, cloak individual banks, and mask deferred error interrupts from each bank. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Core Performance Boost	Enable/Disable the Core Performance Boost function. Options available: Auto, Disabled. Default setting is Auto .
Global C-State Control	Controls the IO based C-state generation and DF C-states. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Power Supply Idle Control	Configures the Power Supply Idle Control. Options available: Auto, Low Current Idle, Typical Current Idle. Default setting is Auto .
SEV ASID Count	Specifies the maximum valid ASID, which affects the maximum system physical address space. Options available: Auto, 253 ASIDs, 509 ASIDs. Default setting is Auto .

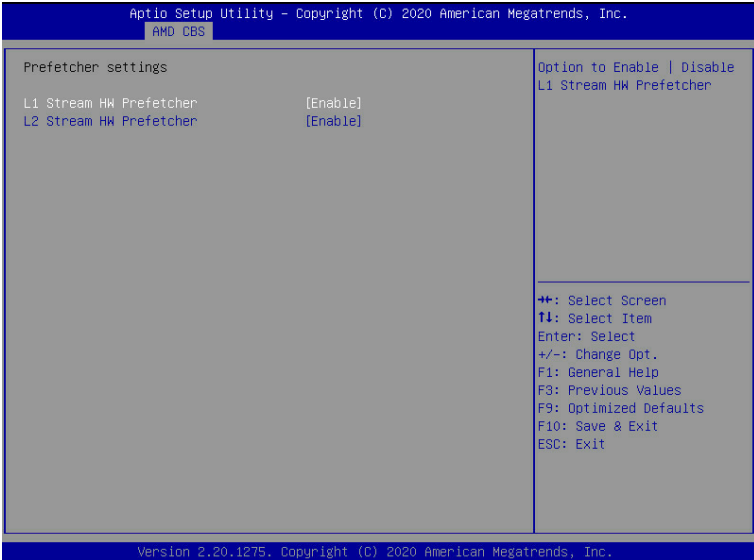
Parameter	Description
SEV-ES ASID Space Limit Control	Space limit control for SEV-ES ASIDs. Options available: Auto, Manual. Default setting is Auto .
Streaming Stores Control	Enable/Disable the Streaming Stores functionality. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Local APIC Mode	Sets the Local APIC Mode. Options available: Auto, xAPIC, x2APIC. Default setting is Auto .
ACPI_CST C1 Declaration	Determines whether or not to declare the C1 state to the OS. Options available: Auto, Enabled, Disabled. Default setting is Auto .
MCA error thresh enable	Enable MCA error thresholding. Options available: Auto, False, True. Default setting is Auto .
SMU and PSP Debug Mode	When this option is enabled, specific uncorrected errors detected by the PSP FW or SMU FW will hand and not reset the system. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Xtrig7 Workaround	Options available: Auto, No Workaround, Bronze Workaround, Sliver Workaround. Default setting is Auto .
PPIN Opt-in	Enable/Disable the PPIN feature. Options available: Auto, Enabled, Disabled. Default setting is Auto .
RdRand	Enable/Disable RdRand instruction. Options available: Auto, Enable, Disable. Default setting is Auto .

5-3-1-1 Performance



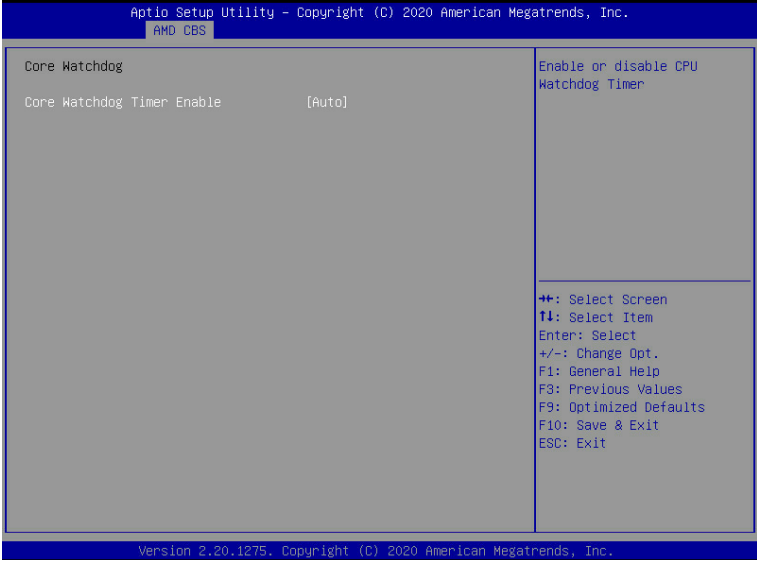
Parameter	Description
Performance	
Custom Core Pstates	<p>Allows you to accept or decline enabling Custom Core Pstates. When accepted, you can disable or customize core Pstates.</p>
CCD/Core/Thread Enablement	<p>Allows you to accept or decline enabling CCDs, processor cores and threads. When accepted, you can control the number of CCDs to be used, the number of cores to be used, and whether to enable or disable Symmetric Multithreading Technology (SMT) support.</p> <ul style="list-style-type: none"> ◆ CCD Control <ul style="list-style-type: none"> – Options available: Auto, 2 CCDs, 3 CCDs, 4 CCDs, 6 CCDs. Default setting is Auto. ◆ Core Control <ul style="list-style-type: none"> – Options available: Auto, TWO(1+1), FOUR(2+2), SIX(3+3). Default setting is Auto. ◆ SMT Control <ul style="list-style-type: none"> – Disable: Single hardware thread per core. – Auto: Two hardware threads per core. – Options available: Disable, Auto. Default setting is Auto.

5-3-1-2 Prefetcher Settings



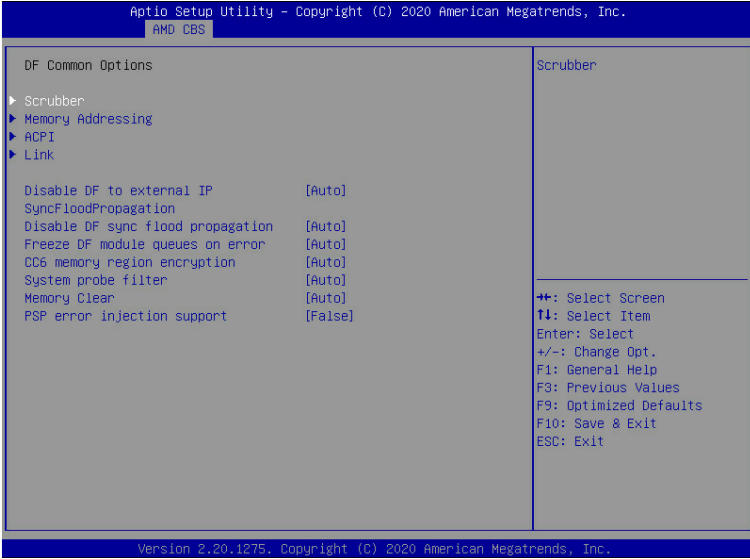
Parameter	Description
Prefetcher settings	
L1 Stream HW Prefetcher	Enable/Disable L1 Stream HW Prefetcher. Options available: Auto, Enable, Disable. Default setting is Auto .
L2 Stream HW Prefetcher	Enable/Disable L2 Stream HW Prefetcher. Options available: Auto, Enable, Disable. Default setting is Auto .

5-3-1-3 Core Watchdog



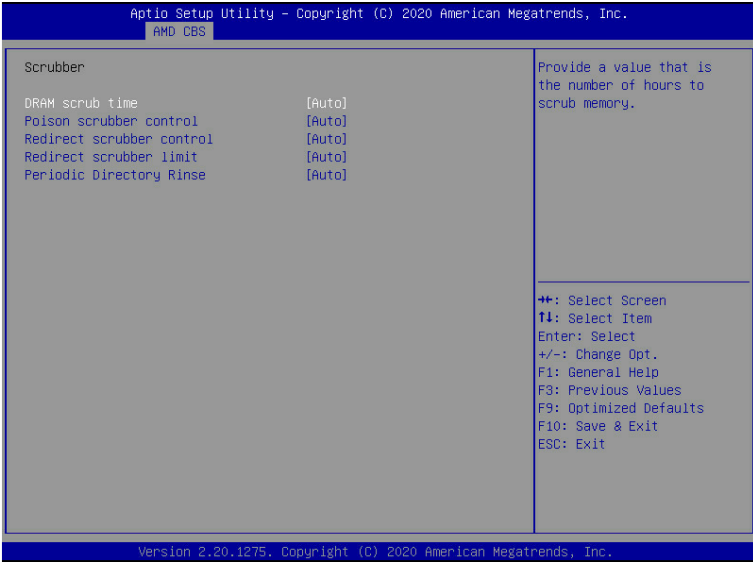
Parameter	Description
Core Watchdog	
Core Watchdog Timer Enable	Enable/Disable CPU Watchdog Timer. Options available: Auto, Enabled, Disabled. Default setting is Auto .

5-3-2 DF Common Options



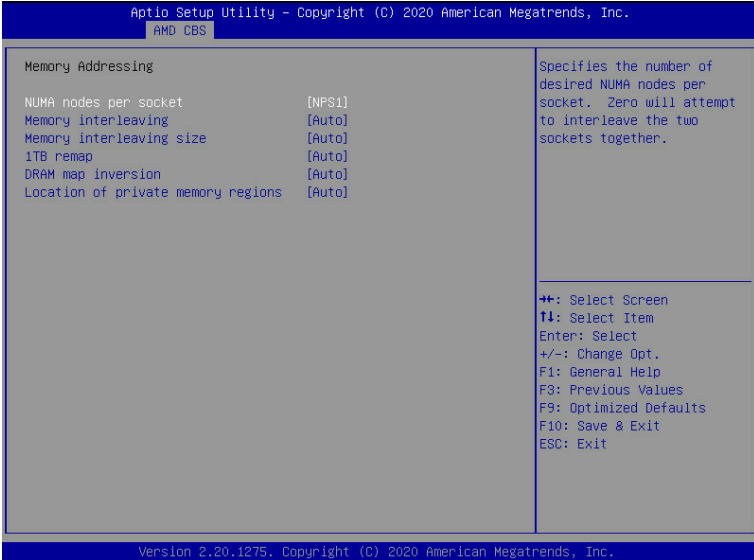
Parameter	Description
DF Common Options	
Scrubber	Press [Enter] for configuration of advanced items.
Memory Addressing	Press [Enter] for configuration of advanced items.
ACPI	Press [Enter] for configuration of advanced items.
Link	Press [Enter] for configuration of advanced items.
Disable DF to external IP sync flood propagation	Enable/Disable SyncFlood to UMC & downstream slaves. Options available: Auto, Sync flood disabled, Sync flood enabled. Default setting is Auto .
Disable DF sync flood propagation	Enable/Disable DF Sync Flood propagation. Options available: Auto, Sync flood disabled, Sync flood enabled. Default setting is Auto .
Freeze DF module queues on error	Options available: Auto, Enabled, Disabled. Default setting is Auto .
CC6 memory region encryption	Controls whether or not the CC6 save/restor memory is encrypted. Options available: Auto, Enabled, Disabled. Default setting is Auto .
System probe filter	Enable/Disable System probe filter. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Memory Clear	Enable/Disable the Memory Clear feature. Options available: Auto, Enabled, Disabled. Default setting is Auto .
PSP error injection support	Enable/Disable PSP error injection support. Options available: False, True. Default setting is False .

5-3-2-1 Scrubber



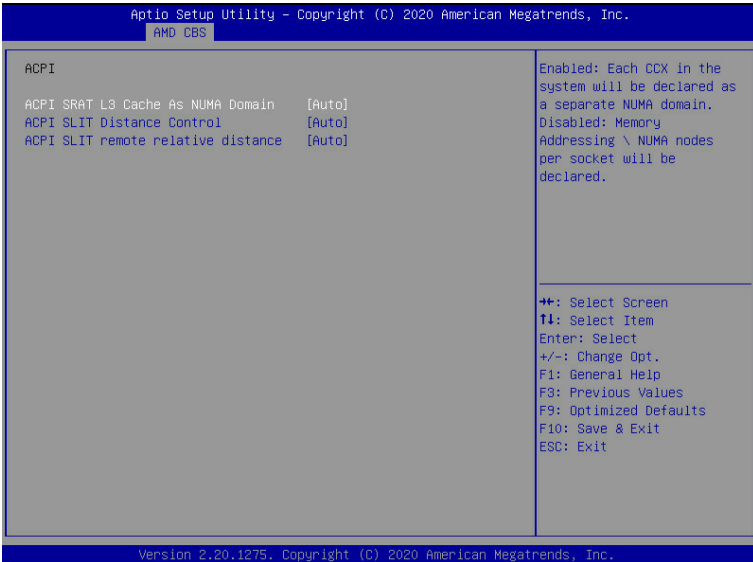
Parameter	Description
Scrubber	
DRAM scrub time	Provide a value that is the number of hours to scrub memory. Options available: Auto, Disabled, 1 hour, 4 hours, 8 hours, 16 hours, 24 hours, 48 hours. Default setting is Auto .
Poison scrubber control	Enable/Disable the Poison scrubber control feature. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Redirect scrubber control	Enable/Disable the Redirect scrubber control feature. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Redirect scrubber limit	Sets the redirect scrubber limit. Options available: Auto, 2, 4, 8, Infinite. Default setting is Auto .
Periodic Directory Rinse	Enable/Disable the Periodic Directory Rinse mode which may help manage directory capacity more efficiently. Options available: Auto, Enabled, Disabled. Default setting is Auto .

5-3-2-2 Memory Addressing



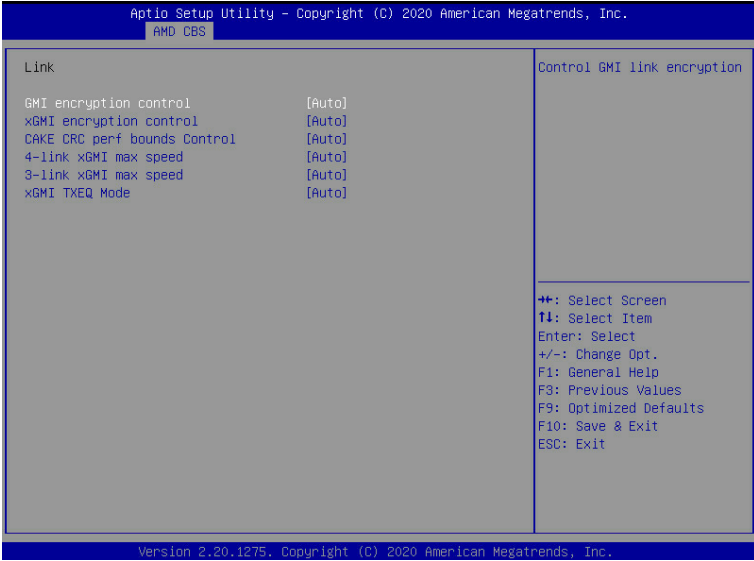
Parameter	Description
Memory Addressing	
NUMA nodes per socket	Specifies the number of desired NUMA nodes per socket. Options available: Auto, NPS0, NPS1, NPS2, NPS4. Default setting is Auto .
Memory interleaving	Enable/Disable the Memory interleaving feature. Options available: Auto, Disabled. Default setting is Auto .
Memory interleaving size	Controls the memory interleaving size. This determines the starting address of the interleave (bit 8, 9, 10 or 11). Options available: Auto, 256Bytes, 512Bytes, 1KB, 2KB. Default setting is Auto .
1TB remap	Enable/Disable to remap DRAM out of the space just below the 1TB boundary. The ability to remap depends on DRAM configuration, NPS, and interleaving selection, and may not always be possible. Options available: Auto, Do not remap, Attempt to remap. Default setting is Auto .
DRAM map inversion	Enable/Disable the DRAM map inversion function. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Location of private memory regions	Controls whether or not the private memory regions (PSP, SMU and CC6) are at the top of DRAM or distributed. Options available: Auto, Distributed, Consolidated. Default setting is Auto .

5-3-2-3 ACPI



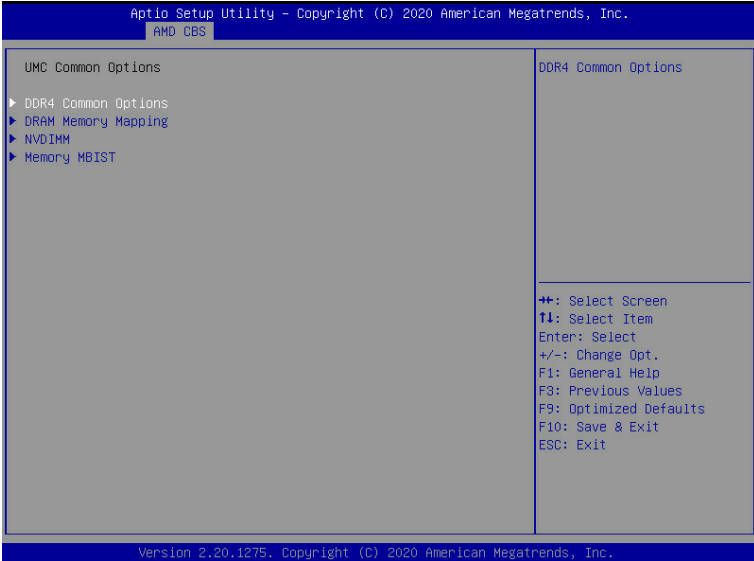
Parameter	Description
ACPI	
ACPI SRAT L3 Cache As NUMA Domain	Enable/Disable report each L3 cache as a NUMA Domain to the OS. Options available: Auto, Enabled, Disabled. Default setting is Auto .
ACPI SLIT Distance Control	Determines how the SLIT distances are declared. Options available: Auto, Manual. Default setting is Auto .
ACPI SLIT remote relative distance	Sets the remote socket distance for 2P systems as near (2.8) or far (3.2). Options available: Auto, Near, Far. Default setting is Auto .

5-3-2-4 Link



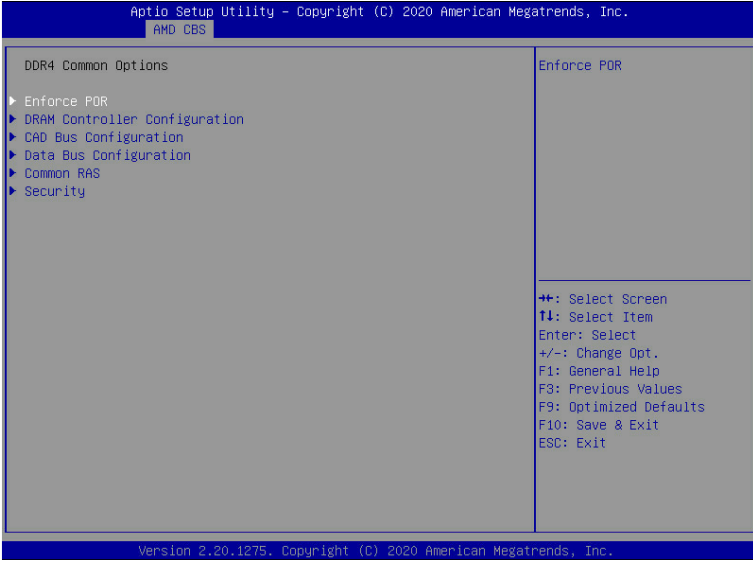
Parameter	Description
Link	
GMI encryption control	Enable/Disable GMI link encryption. Options available: Auto, Enabled, Disabled. Default setting is Auto .
xGMI encryption control	Enable/Disable xGMI link encryption. Options available: Auto, Enabled, Disabled. Default setting is Auto .
CAKE CRC perf bounds Control	Options available: Auto, Manual. Default setting is Auto .
4-link xGMI max speed	Specifies the max speed of 4-link xGMI. Options available: Auto, 10.667Gbps, 13Gbps, 16Gbps, 18Gbps. Default setting is 10.667Gbps .
3-link xGMI max speed	Specifies the max speed of 3-link xGMI. Options available: Auto, 10.667Gbps, 13Gbps, 16Gbps, 18Gbps. Default setting is 10.667Gbps .
xGMI TXEQ Mode	Configures xGMI TXEQ/RX vetting Mode. Options available: Auto, TXEQ_Disabled, TXEQ_Lane, TXEQ_Link, TXEQ_RX_Vet. Default setting is Auto .

5-3-3 UMC Common Options



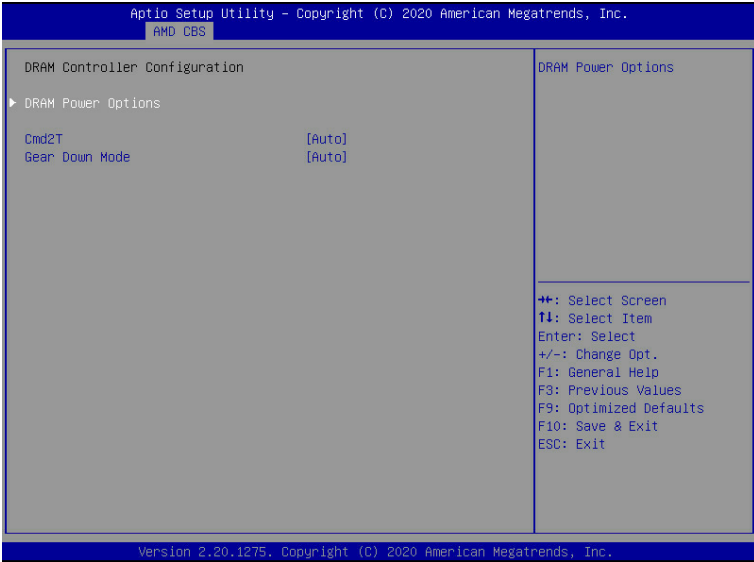
Parameter	Description
UMC Common Options	
DDR4 Common Options	Press [Enter] for configuration of advanced items.
DRAM Memory Mapping	Press [Enter] for configuration of advanced items.
NVDIMM	Press [Enter] for configuration of advanced items.
Memory MBIST	Press [Enter] for configuration of advanced items.

5-3-3-1 DDR4 Common Options



Parameter	Description
DDR4 Common Options	
Enforce POR	<p>Press [Enter] to configure the Plan of Record (POR) to enable / disable restrictions for DDR4 frequency and voltage programming. Memory speeds will be capped at AMD guidelines.</p> <ul style="list-style-type: none"> ◆ Decline ◆ Accept – Overclock <ul style="list-style-type: none"> » Enable/Disable Memory Overclock Settings » Options available: Auto, Enabled. Default setting is Auto.
DRAM Controller Configuration	Press [Enter] to configure DRAM Controller Configuration.
CAD Bus Configuration	Press [Enter] to configure CAD Bus Configuration.
Data Bus Configuration	Press [Enter] to configure Data Bus Configuration.
Common RAS	Press [Enter] to configure Common RAS.
Security	Press [Enter] to configure Security.

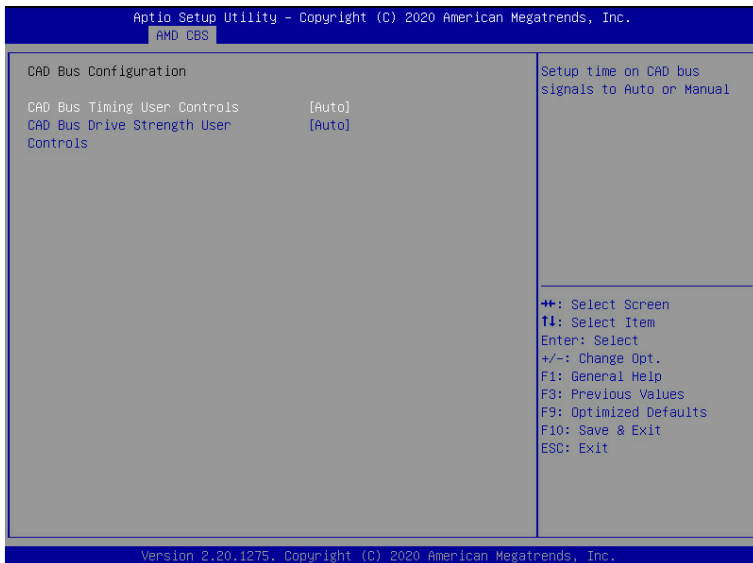
5-3-3-1-1 DRAM Controller Configuration



Parameter	Description
DRAM Controller Configuration	
DRAM Power Options	<p>Press [Enter] to configure DRAM Power Options.</p> <ul style="list-style-type: none"> ◆ Power Down Enable <ul style="list-style-type: none"> – Enable/Disable DDR power down mode. – Options available: Auto, Enabled, Disabled. Default setting is Auto. ◆ SubUrgRefLowerBound <ul style="list-style-type: none"> – Specifies the stored refresh limit to required enter sub-urgent refresh mode. Valid value: 6~1. – Default setting is 4. ◆ UrgRefLimit <ul style="list-style-type: none"> – Specifies the stored refresh limit to required enter urgent refresh mode. Valid value: 6~1. – Default setting is 6. ◆ DRAM Maximum Activate Count <ul style="list-style-type: none"> – Options available: Untested MAC, 700K, 600K, 500K, 400K, 300K, 200K, Unlimited MAC, Auto. Default setting is Auto. ◆ DRAM Refresh Rate <ul style="list-style-type: none"> – Options available: 7.8 usec, 3.9 usec. Default setting is 7.8 usec. ◆ Self-Refresh Exit Staggering <ul style="list-style-type: none"> – Options available: Disabled, Trfc/3, Trfc/4. Default setting is Disabled.
Cmd2T	<p>Selects the Cmd2T mode on ADDR/CMD.</p> <p>Options available: Auto, 1T, 2T. Default setting is Auto.</p>

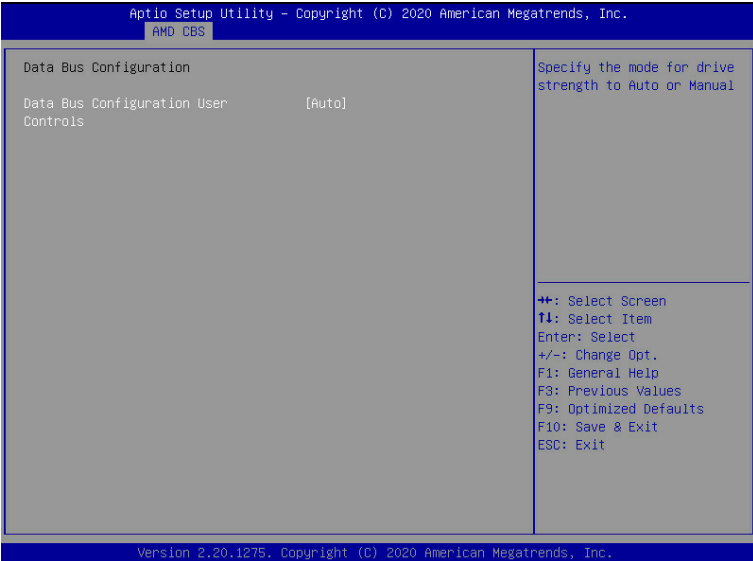
Parameter	Description
Gear Down Mode	Enable/Disable the Gear Down Mode function. Options available: Auto, Enabled, Disabled. Default setting is Auto .

5-3-3-1-2 CAD Bus Configuration



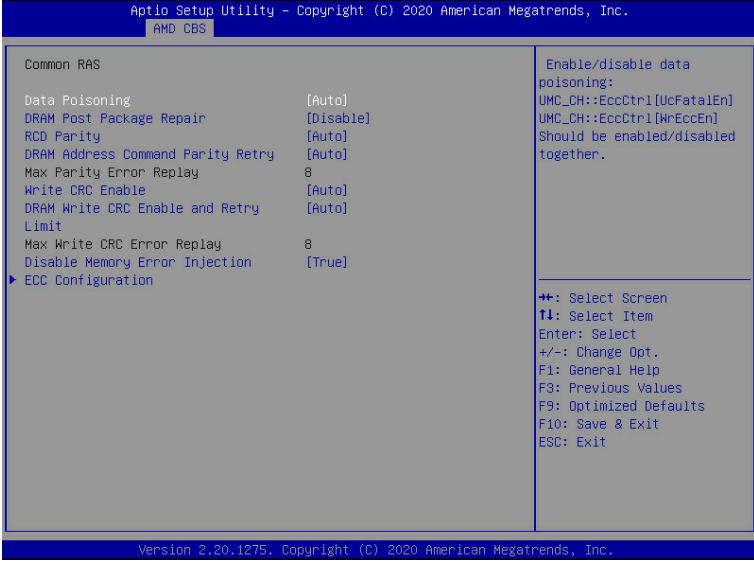
Parameter	Description
CAD Bus Configuration	
CAD Bus Timing User Controls	Setup time on CAD bus signals to Auto or Manual. Options available: Auto, Manual. Default setting is Auto .
CAD Bus Drive Strength User Controls	Drive Strength on CAD bus signals to Auto or Manual. Options available: Auto, Manual. Default setting is Auto .

5-3-3-1-3 Data Bus Configuration



Parameter	Description
Data Bus Configuration	
Data Bus Configuration User Controls	Specifies the mode for drive strength to Auto or Manual. Options available: Auto, Manual. Default setting is Auto .

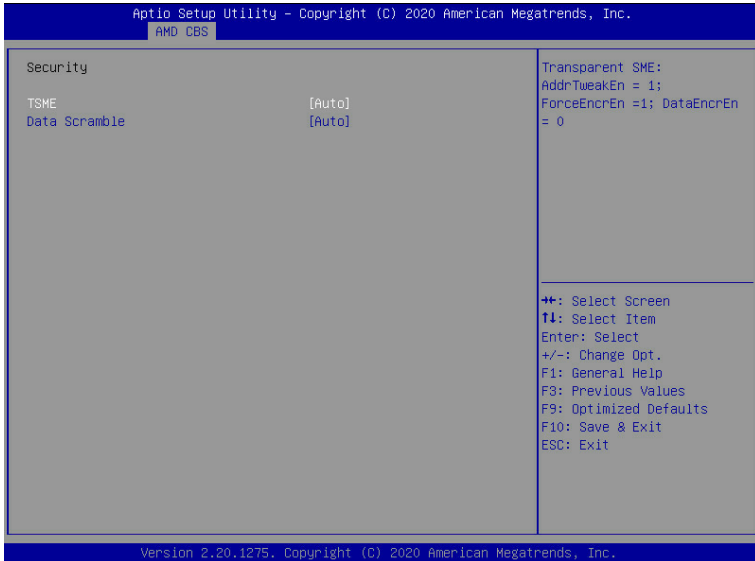
5-3-3-1-4 Common RAS



Parameter	Description
Common RAS	
Data Poisoning	Enable/Disable the Data Poisoning function. Options available: Auto, Enabled, Disabled. Default setting is Auto .
DRAM Post Package Repair	Enable/Disable the DRAM Post Package Repair function. Options available: Enable, Disable. Default setting is Disable .
RCD Parity	Enable/Disable the RCD Parity function. Options available: Auto, Enabled, Disabled. Default setting is Auto .
DRAM Address Command Parity Retry	Enable/Disable the DRAM Address Command Parity Retry function. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Max Parity Error Replay	Configures the Max Parity Error Replay. (0-0x3f) Default setting is 8 . Please note that this item is configurable when DRAM Address Command Parity Retry is set to Enabled.
Write CRC Enable	Enable/Disable the Write CRC function. Options available: Auto, Enabled, Disabled. Default setting is Auto .
DRAM Write CRC Enable and Retry Limit	Enable/Disable DRAM Write CRC Enable and Retry Limit. Options available: Auto, Enabled, Disabled. Default setting is Auto . Configures the Max Write CRC Error Replay. (0-0x3f)
Max Write CRC Error Replay	Default setting is 8 . Please note that this item is configurable when DRAM Write CRC Enable and Retry Limit is set to Enabled.

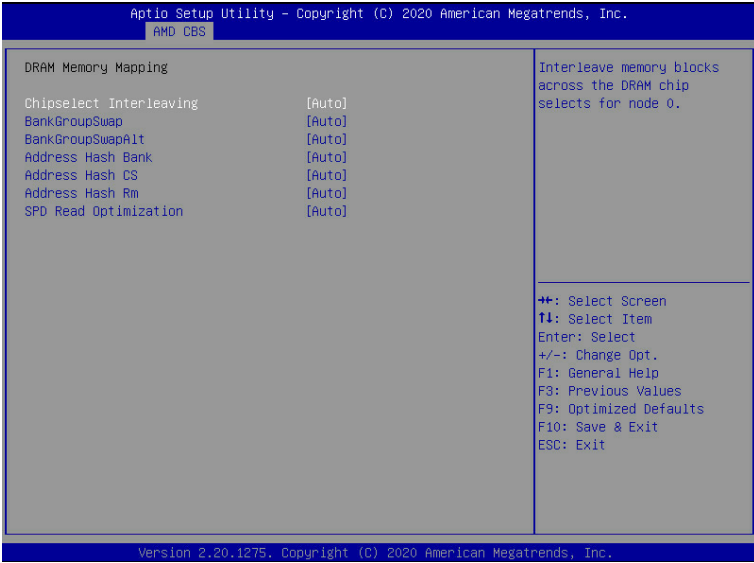
Parameter	Description
Disable Memory Error Injection	Options available: False, True. Default setting is True .
ECC Configuration	<p data-bbox="396 189 732 213">Press [Enter] to configure advanced items.</p> <ul style="list-style-type: none"> <li data-bbox="396 221 954 299">◆ DRAM ECC Symbol Size <ul style="list-style-type: none"> <li data-bbox="434 247 783 271">– Configures the DRAM ECC Symbol Size. <li data-bbox="434 272 926 296">– Options available: Auto, x4, x8, x16. Default setting is Auto. <li data-bbox="396 307 954 417">◆ DRAM ECC Enable <ul style="list-style-type: none"> <li data-bbox="434 333 942 388">– Enable/Disable DRAM ECC. When set to Auto, it will set ECC to enable. <li data-bbox="434 393 954 448">– Options available: Auto, Enabled, Disabled. Default setting is Auto. <li data-bbox="396 453 954 561">◆ DRAM UECC Retry <ul style="list-style-type: none"> <li data-bbox="434 479 742 503">– Enable/Disable DRAM UECC Retry. <li data-bbox="434 508 954 561">– Options available: Auto, Enabled, Disabled. Default setting is Auto.

5-3-3-1-5 Security



Parameter	Description
Security	
TSME	Enable/Disable transparent secure memory encryption. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Data Scramble	Enable/Disable Data Scrambling. Options available: Auto, Enabled, Disabled. Default setting is Auto .

5-3-3-2 DRAM Memory Mapping



Parameter	Description
DRAM Memory Mapping	
Chipselect Interleaving	Interleave memory blocks across the DRAM chip selects for node 0. Options available: Auto, Disabled. Default setting is Auto .
BankGroupSwap	Configures the BankGroupSwap. BankGroupSwap (BGS) is a new memory mapping option in AGESA that alters how applications get assigned to physical locations within the memory modules. When this option sets to Auto, it is null: No help string. Options available: Auto, Enabled, Disabled. Default setting is Auto .
BankGroupSwapAlt	Configures the BankGroupSwapAlt. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Address Hash Bank	Enable/Disable bank address hashing. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Address Hash CS	Enable/Disable CS address hashing. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Address Hash Rm	Enable/Disable RM address hashing. Options available: Auto, Enabled, Disabled. Default setting is Auto .
SPD Read Optimization	Enable/Disable SPD Read Optimization. Options available: Auto, Enabled, Disabled. Default setting is Auto .

5-3-3-3 NVDIMM



Parameter	Description
NVDIMM	Displays the information of the devices/controllers if installed
Disable NVDIMM-N Feature	Enable/Disable NVDIMM-N feature for memory margin tool. Options available: No, Yes. Default setting is NO .

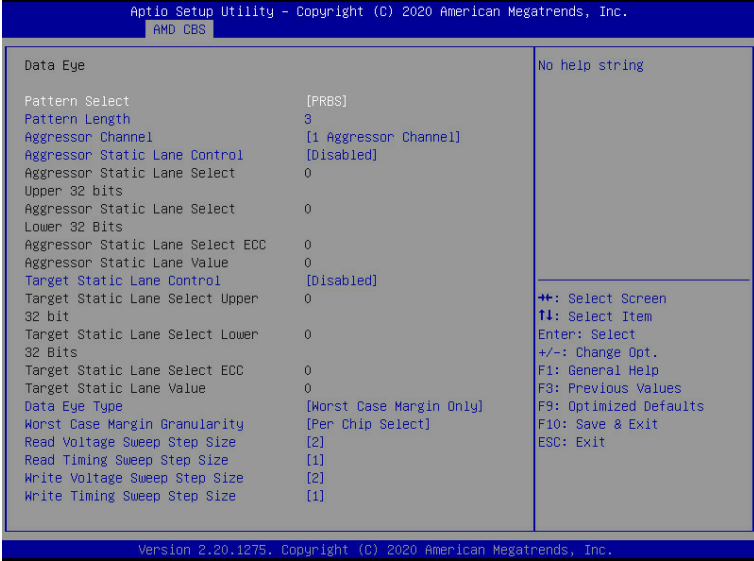
5-3-3-4 Memory MBIST



Parameter	Description
Memory MBIST	
MBIST Enable	Enable/Disable the Memory MBIST function. Options available: Enabled, Disabled. Default setting is Disabled .
MBIST Test Mode ^(Note)	Selects MBIST Test Mode. Interface Mode: Tests Single and Multiple CS transactions and Basic Connectivity. Data Eye Mode: Measures Voltage vs. Timing. Options available: Auto, Both, Interface Mode, Data Eye Mode. Default setting is Auto .
MBIST Aggressors ^(Note)	Enable/Disable MBIST Aggressor test. Options available: Auto, Enabled, Disabled. Default setting is Auto .
MBIST Per Bit Slave Die Reporting ^(Note)	Enable/Disable to report 2D data eye results in ABL log for each DQ, Chipselect, and Channel. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Data Eye	Press [Enter] to configure advanced items.

(Note) This item is available when **MBIST Enable** is set to **Enabled**.

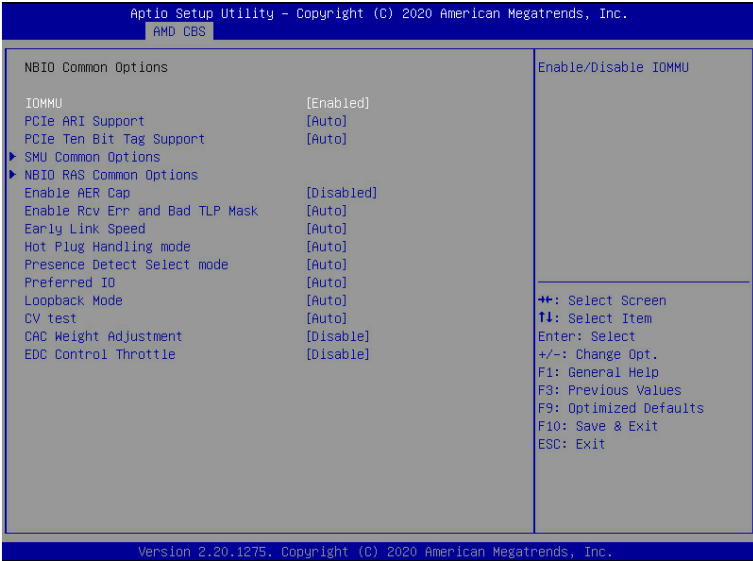
5-3-3-4-1 Data Eye



Parameter	Description
Data Eye	
Pattern Select	Options available: PRBS, SSO, Both. Default setting is PRBS .
Pattern Length	Determines the pattern length. The possible options are N=3....12.
Aggressor Channel	This item helps read the aggressors channels. Options available: Disabled, 1 Aggressor Channel, 3 Aggressor Channels, 7 Aggressor Channels. Default setting is 1 Aggressor Channel .
Aggressor Static Lane Control	Enable/Disable the Aggressor Static Lane Control function. Options available: Enabled, Disabled. Default setting is Disabled .
Aggressor Static Lane Select Upper 32 bits	This item is configurable when Aggressor Static Lane Control is set to Enabled .
Aggressor Static Lane Select Lower 32 bits	This item is configurable when Aggressor Static Lane Control is set to Enabled .
Aggressor Static Lane Select ECC	This item is configurable when Aggressor Static Lane Control is set to Enabled .
Aggressor Static Lane Value	This item is configurable when Aggressor Static Lane Control is set to Enabled .
Target Static Lane Control	Enable/Disable the Target Static Lane Control function. Options available: Enabled, Disabled. Default setting is Disabled .

Parameter	Description
Target Static Lane Select Upper 32 bits	This item is configurable when Target Static Lane Control is set to Enabled .
Target Static Lane Select Lower 32 bits	This item is configurable when Target Static Lane Control is set to Enabled .
Target Static Lane Select ECC	This item is configurable when Target Static Lane Control is set to Enabled .
Target Static Lane Value	This item is configurable when Target Static Lane Control is set to Enabled .
Data Eye Type	This item determines which results are expected to be captured for Data Eye. Options available: 1D Voltage Sweep, 1D Timing Sweep, 2D Full Data Eye, Worst Case Margin Only. Default setting is Worst Case Margin Only .
Worst Case Margin Granularity	Configures Worst Case Margin Granularity. Options available: Per Chip Select, Per Nibble. Default setting is Per Chip Select .
Read Voltage Sweep Step Size	Configures the step size for read Data Eye voltage sweep. Options available: 1, 2, 4. Default setting is 2 .
Read Timing Sweep Step Size	Configures the step size for read Data Eye timing sweep. Options available: 1, 2, 4. Default setting is 1 .
Write Voltage Sweep Step Size	Configures the step size for write Data Eye voltage sweep. Options available: 1, 2, 4. Default setting is 2 .
Write Timing Sweep Step Size	Configures the step size for write Data Eye timing sweep. Options available: 1, 2, 4. Default setting is 1 .

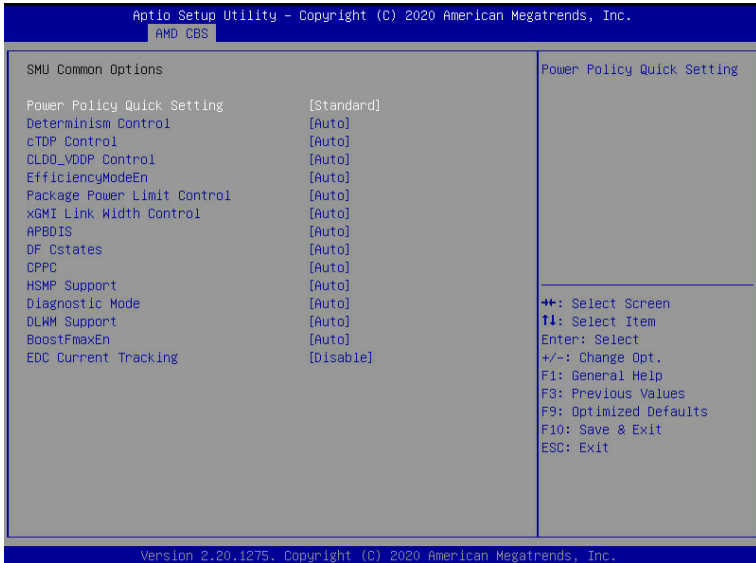
5-3-4 NBIO Common Options



Parameter	Description
NBIO Common Options	
IOMMU	Enable/Disable the IOMMU function. Options available: Enabled, Disabled. Default setting is Disabled .
PCIe ARI Support	Enable/Disable Alternative Routing-ID Interpretation. Options available: Auto, Enabled, Disabled. Default setting is Auto .
PCIe Ten Bit Tag Support	Enable/Disable PCIe ten bit tags for supported devices. (Auto=Disabled) Options available: Auto, Enabled, Disabled. Default setting is Auto .
SMU Common Options	Press [Enter] for configuration of advanced items.
NBIO RAS Common Options	Press [Enter] for configuration of advanced items.
Enable AER Cap	Enable/Disable Advanced Error Reporting Capability. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Enable Rcv Err and Bad TLP Mask	Enable/Disable Masking of Receiver Error and Bad TLP at Gen4 x2. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Early Link Speed	Configures Early Link Speed. Options available: Auto, Gen1, Gen2. Default setting is Auto .

Parameter	Description
Hot Plug Handling mode	Controls the Hot Plug Handling mode. Options available: Auto, A0 Mode, OS First (No Error Handling), OS First (Error Handling-Not Implemented), Firmware First (Not Implemented). Default setting is Auto .
Presence Detect Select mode	Controls the Presence Detect Select mode. Options available: Auto, OR, AND. Default setting is Auto .
Preferred IO	Preferred IO select type. Manual: Bus Number manually. Auto: Default. Options available: Auto, Manual. Default setting is Auto .
Loopback Mode	Enable/Disable the PCIe loopback mode. Options available: Auto, Enabled, Disabled. Default setting is Auto .
CV test	Enable/Disable the running PCIECV tool support. Options available: Auto, Enabled, Disabled. Default setting is Auto .
CAC Weight Adjustment	Enable/Disable the EDC Mode Select. Options available: Auto, Enable, Disable. Default setting is Disable .
EDC Control Throttle	Enable/Disable the EDC Control Throttle. Options available: Auto, Enable, Disable. Default setting is Disable .

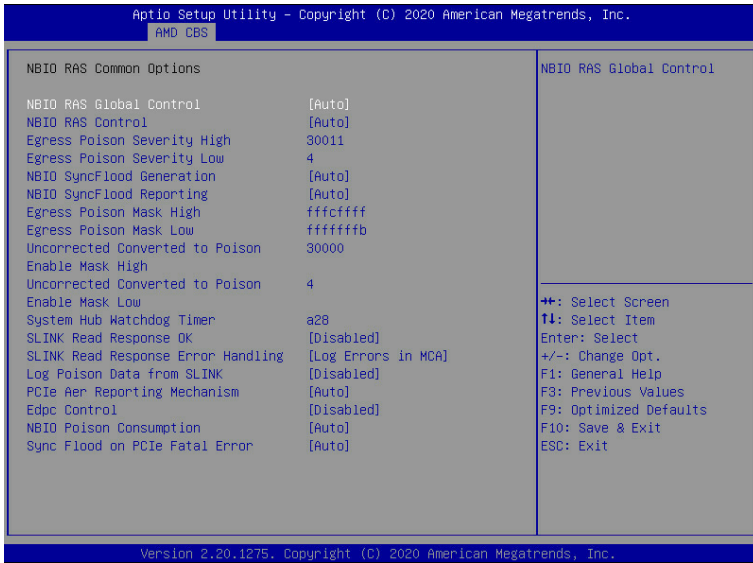
5-3-4-1 SMU Common Options



Parameter	Description
SMU Common Options	
Power Policy Quick Setting	Options available: Standard, Best Performance, Energy Efficient. Default setting is Standard .
Determinism Control	Selects use the fused Determinism or set customized Determinism. Options available: Auto, Manual. Default setting is Auto .
cTDP Control	Selects use the fused TDP or set customized TDP. **TDP is used to define the RC thermal model only** Options available: Auto, Manual. Default setting is Auto .
CLDD_VDDP Control	Options available: Auto, Manual. Default setting is Auto .
EfficiencyModeEn	Options available: Auto, Enabled. Default setting is Auto .
Package Power Limit Control	Selects use the fused PPT or set customized PPT. **PPT will be used as the ASIC power limit** Options available: Auto, Manual. Default setting is Auto .
xGMI Link Width Control	Options available: Auto, Manual. Default setting is Auto .
APBDIS	Options available: Auto, 0, 1. Default setting is Auto .
DF Cstates	Enable/Disable DF C-states. Options available: Auto, Enabled, Disabled. Default setting is Auto .

Parameter	Description
CPPC	Enable/Disable the CPPC feature. Options available: Auto, Enabled, Disabled. Default setting is Auto .
HSMP Support	Enable/Disable the HSMP support. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Diagnostic Mode	Enable/Disable the Diagnostic Mode. Options available: Auto, Enabled, Disabled. Default setting is Auto .
DLWM Support	Enable/Disable the DLWM support. Options available: Auto, Enabled, Disabled. Default setting is Auto .
BoostFmaxEn	Options available: Auto, Manual. Default setting is Auto .
EDC Current Tracking	The generation a correctable MCE when the telemetry current value is over the set threshold defined by EDC Current Tracking Current Threshold. Options available: Enable, Disable. Default setting is Disable .

5-3-4-2 NBIO RAS Common Options



Parameter	Description
NBIO RAS Common Options	
NBIO RAS Global Control	Options available: Auto, Manual. Default setting is Auto .
NBIO RAS Control	Options available: Disabled, MCA, Legacy, Auto. Default setting is Auto .
Egress Poison Severity High	Configures the Egress Poison High Severity. Each bit set to 1 enables High severity on the associated IOHC egress port. A bit of 0 indicates LOW severity.
Egress Poison Severity Low	Configures the Egress Poison Low Severity. Each bit set to 1 enables High severity on the associated IOHC egress port. A bit of 0 indicates LOW severity.
NBIO SyncFlood Generation	The value may be used to mask SyncFlood caused by NBIO RAS options. Options available: Auto, Enabled, Disabled. Default setting is Auto .
NBIO SyncFlood Reporting	The value may be used to enable SyncFlood reporting to APML. Options available: Enabled, Disabled. Default setting is Disabled .
Egress Poison Mask High	Enables mask for masking of errors logged in EGRESS_POISON_STATUS. For each bit set to 1, errors are masked. For each bit set to 0, errors trigger response actions.
Egress Poison Mask Low	Enables mask for masking of errors logged in EGRESS_POISON_STATUS. For each bit set to 1, errors are masked. For each bit set to 0, errors trigger response actions.

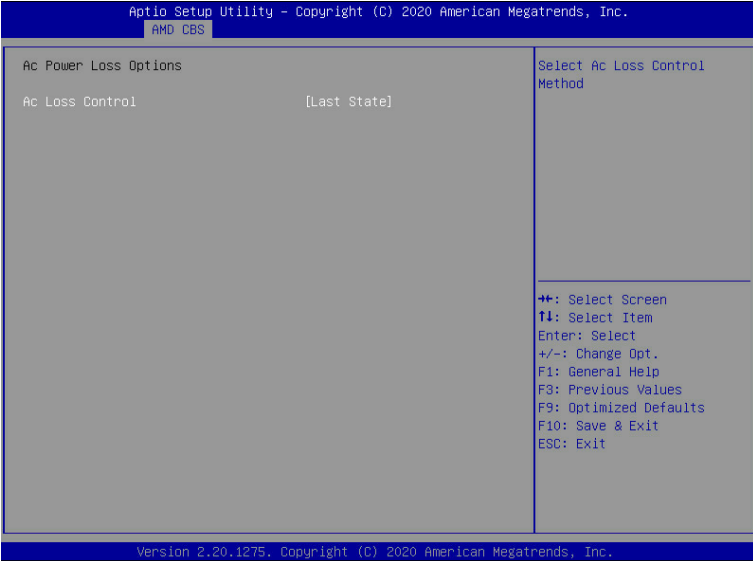
Parameter	Description
Uncorrected Converted to Poison Enable Mask High	Enables mask for masking of uncorrectable parity errors on internal arrays.
Uncorrected Converted to Poison Enable Mask Low	Enables mask for masking of uncorrectable parity errors on internal arrays.
System Hub Watchdog Timer	Specifies the timer interval of the SYSHUB Watchdog timer in milliseconds.
SLINK Read Response OK	This item specifies whether SLINK read response errors are converted to an Okay response. Options available: Enabled, Disabled. Default setting is Disabled .
SLINK Read Response Error Handling	Options available: Enabled, Trigger MCOMMIT Error, Log Errors in MCA. Default setting is Log Errors in MCA .
Log Poison Data from SLINK	Enable/Disable the Log Poison Data from SLINK feature. Options available: Enabled, Disabled. Default setting is Disabled .
PCIe Aer Reporting Mechanism	Selects the method of reporting AER errors from PCI Express. Options available: Auto, Firmware First, OS First, MCA. Default setting is Auto .
Edpc Control	Options available: Auto, Enabled, Disabled. Default setting is Disabled .
NBIO Poison Consumption	Options available: Auto, Enabled, Disabled. Default setting is Auto .
Sync Flood on PCIe Fatal Error	Options available: Auto, True, False. Default setting is Auto .

5-3-5 FCH Common Options



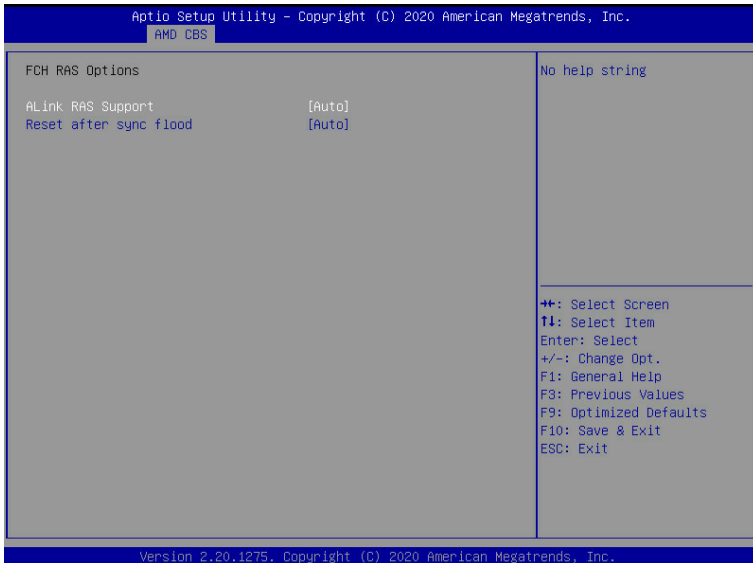
Parameter	Description
FCH Common Options	
AC Power Loss Options	Press [Enter] for configuration of advanced items.
FCH RAS Options	Press [Enter] for configuration of advanced items.
Miscellaneous Options	Press [Enter] for configuration of advanced items.

5-3-5-1 AC Power Loss Options



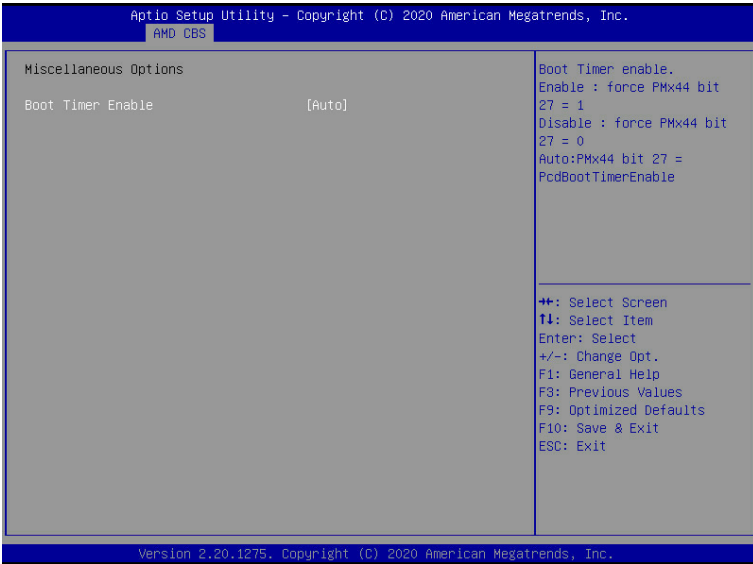
Parameter	Description
AC Power Loss Options	
AC Loss Control	Selects the AC Loss Control Method. Options available: Power Off, Power On, Last State. Default setting is Last State .

5-3-5-2 FCH RAS Options



Parameter	Description
FCH RAS Options	
ALink RAS Support	Enable/Disable the ALink RAS Support. Options available: Auto, Enabled, Disabled. Default setting is Auto .
Reset after sync flood	Enables AB to forward downstream sync-flood message to system controller. Options available: Auto, Enabled, Disabled. Default setting is Auto .

5-3-5-3 Miscellaneous Options



Parameter	Description
Miscellaneous Options	
Boot Timer Enable	Enable/Disable the Boot Timer Options available: Auto, Enabled, Disabled. Default setting is Auto .

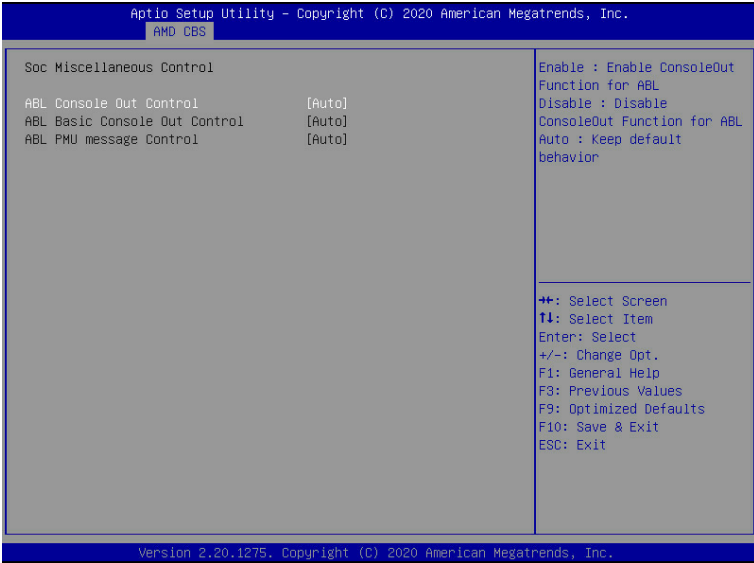
5-3-6 NTB Common Options



Parameter	Description
NTB Common Options	
NTB Enable	Options available: Auto, Enable. Default setting is Auto .
NTB Location ^(Note)	Specifies the NTB location. Default setting is Auto .
NTB active on PCIeCore ^(Note)	NTB enable on PCIe Core. Options available: Auto, Core0, Core1. Default setting is Auto .
NTB Mode ^(Note)	Selects the NTB Mode. Options available: Auto, NTB Disabled, NTB Primary, NTB Secondary, NTB Random. Default setting is Auto .
Link Speed ^(Note)	Selects Link Speed for NTB Mode. Options available: Auto, Max Speed, Gen1, Gen2, Gen3, Gen4. Default setting is Auto .

(Note) This item appears when **NTB Enable** is set to **Enable**.

5-3-7 SOC Miscellaneous Control



Parameter	Description
SOC Miscellaneous Control	
ABL Console Out Control	Enable/Disable the ConsoleOut function for ABL. Options available: Auto, Enable, Disable. Default setting is Auto .
ABL Basic Console Out Control ^(Note)	Enable/Disable the Basic ConsoleOut function for ABL. Options available: Auto, Enable, Disable. Default setting is Auto .
ABL PMU message Control ^(Note)	To Control the total number of PMU debug messages. Options available: Auto, Detailed debug message, Coarse debug message, Stage completion, Firmware completion message only. Default setting is Auto .

(Note) This item is configurable when **ABL Console Out Control** is set to **Enabled**.

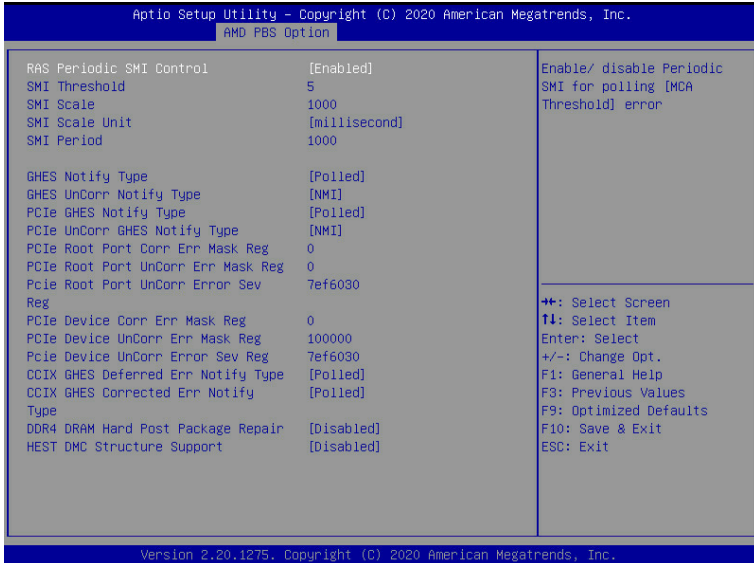
5-4 AMD PBS Menu

AMD PBS Option menu displays submenu options for configuring the function of AMD PBS. Select a submenu item, then press [Enter] to access the related submenu screen.



Parameter	Description
RAS	Press [Enter] for configuration of advanced items.
SPI Locking	Enable/Disable SPI Locking for protect ROM part. Options available: Enabled, Disabled. Default setting is Disabled .

5-4-1 RAS



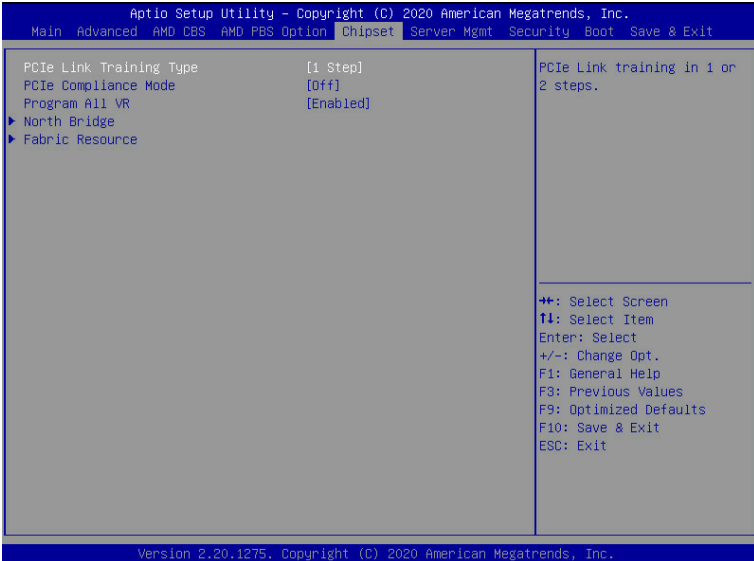
Parameter	Description
RAS Periodic SMI Control	Enable/Disable the Periodic SMI for polling [MCA Threshold] error. Options available: Enabled, Disabled. Default setting is Enabled .
SMI Threshold	Configures the SMI Threshold value.
SMI Scale	Configures the SMI Scale value.
SMI Scale Unit	Defines the unit of time scale. Options available: millisecond, second, minute. Default setting is millisecond .
SMI Period	Configures the SMI Period.
GHES Notify Type	Selects the Notification type for deferred/ corrected errors. Options available: Polled, SCI. Default setting is Polled .
GHES UnCorr Notify Type	Selects the Notification type for uncorrected errors. Options available: Polled, NMI. Default setting is NMI .
PCIe GHES Notify Type	Selects the Notification type for PCIe corrected errors. Options available: Polled, SCI. Default setting is Polled .
PCIe UnCorr GHES Notify Type	Selects the Notification type for PCIe uncorrected errors. Options available: Polled, NMI. Default setting is NMI .
PCIe Root Port Corr Err Mask Reg	Initialize the PCIe AER Corrected Error Mask register of Root Port.

Parameter	Description
PCIe Root Port UnCorr Err Mask Reg	Initialize the PCIe AER Uncorrected Error Mask register of Root Port.
PCIe Root Port UnCorr Err Sev Reg	Initialize the PCIe AER Uncorrected Error Severity register of Root Port.
PCIe Device Corr Err Mask Reg	Initialize the PCIe AER Corrected Error Mask register of PCIe device.
PCIe Device UnCorr Err Mask Reg	Initialize the PCIe AER Uncorrected Error Mask register of PCIe device.
PCIe Device UnCorr Err Sev Reg	Initialize the PCIe AER Uncorrected Error Severity register of PCIe device.
CCIX GHES Deferred ERR Notify Type	Selects the Notification type for CCIX deferred error. Options available: Polled, SCI. Default setting is Polled .
CCIX GHES Corrected Err Notify Type	Selects the Notification type for CCIX corrected error. Options available: Polled, SCI. Default setting is Polled .
DDR4 DRAM Hard Post Package Repair	This feature allows spare DRAM rows to replace malfunctioning rows via an in-field repair mechanism. Options available: Enabled, Disabled. Default setting is Disabled .
HEST DMC Structure Support	HEST DMC (Deferred Machine Check) Structure Support. Options available: Enabled, Disabled. Default setting is Disabled .

5-5 Chipset Setup Menu

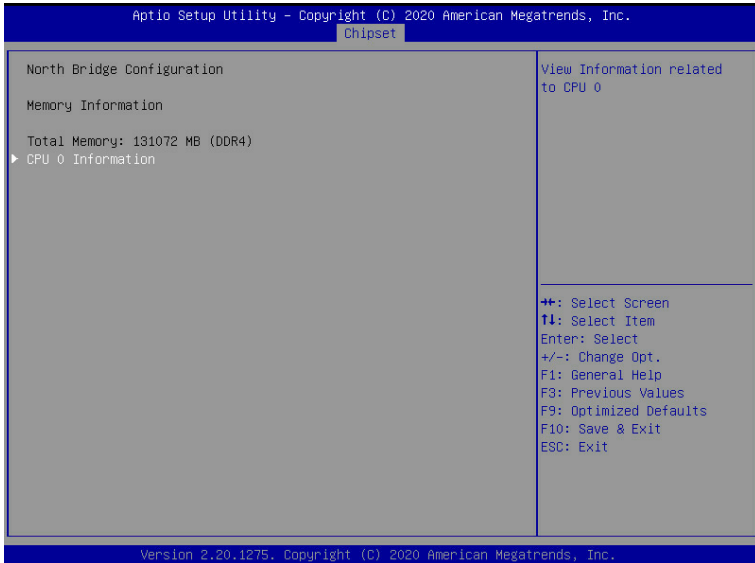
Chipset Setup menu displays submenu options for configuring the function of the South Bridge and North Bridge.

Select a submenu item, then press <Enter> to access the related submenu screen.



Parameter	Description
PCIe Link Training Type	Configures the PCIe Link training in 1 or 2 steps. Options available: 1 Step, 2 Step. Default setting is 1 Step .
PCIe Compliance Mode	Options available: On, Off. Default setting is Off .
Program All VR	Enable/Disable program all VR on MB. Options available: Enabled, Disabled. Default setting is Enabled .
North Bridge	Press [Enter] for configuration of advanced items.
Fabric Resource	Press [Enter] for configuration of advanced items.

5-5-1 North Bridge



Parameter	Description
North Bridge Configuration	
Memory Information	
Total Memory	Displays the total memory information.
CPU 0 Information	Press [Enter] to view information related to CPU 0.

5-5-2 Fabric Resource

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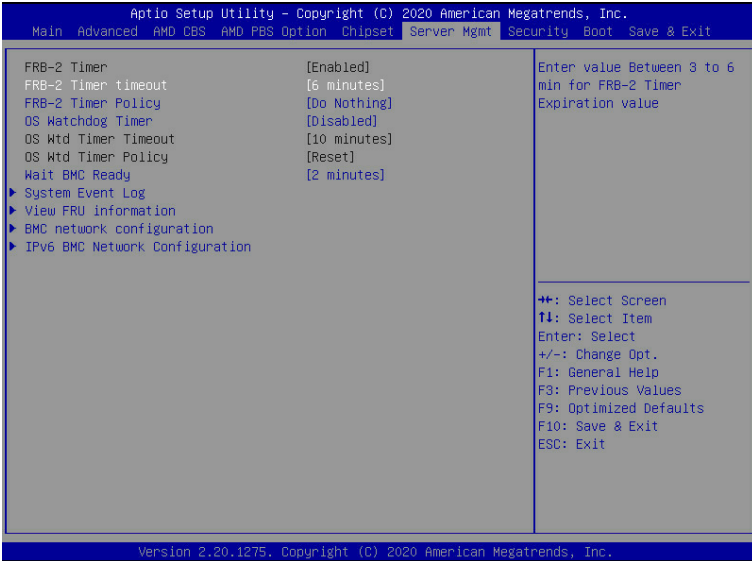
Chipset

<p>Fabric Resource</p> <p>UP0 NBIO0 Base Bus:0xC0 Socket 0 NBIO0 PCIe Bus Number 40</p> <p>UP0 NBIO1 Base Bus:0x80 Socket 0 NBIO0 PCIe Bus Number 40</p> <p>UP0 NBIO2 Base Bus:0x40 Socket 0 NBIO0 PCIe Bus Number 40</p> <p>UP0 NBIO3 Base Bus:0x00 Socket 0 NBIO0 PCIe Bus Number 40</p>	<p>Change Socket 0 NBIO0 PCIe bus number</p> <hr/> <p> ++: Select Screen ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F8: Previous Values F9: Optimized Defaults F10: Save & Exit ESC: Exit </p>
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Parameter	Description
Fabric Resource	
UP0 NBIO# Base Bus	Change Socket NBIO PCIe bus number.

5-6 Server Management Menu



Parameter	Description
FRB-2 Timer	Enable/Disable FRB-2 timer (POST timer). Options available: Enabled, Disabled. Default setting is Enabled .
FRB-2 Timer ^(Note1) timeout	Configures the FRB2 Timer timeout. Options available: 3 minutes, 4 minutes, 5 minutes, 6 minutes. Default setting is 6 minutes .
FRB-2 Timer Policy ^(Note1)	Configures the FRB2 Timer policy. Options available: Do Nothing, Reset, Power Down. Default setting is Do Nothing .
OS Watchdog Timer	Enable/Disable OS Watchdog Timer function. Options available: Enabled, Disabled. Default setting is Disabled .
OS Wtd Timer Timeout ^(Note2)	Configures OS Watchdog Timer. Options available: 5 minutes, 10 minutes, 15 minutes, 20 minutes. Default setting is 10 minutes .
OS Wtd Timer Policy ^(Note2)	Configure OS Watchdog Timer Policy. Options available: Reset, Do Nothing, Power Down. Default setting is Reset .
Wait BMC Ready	Post wait BMC ready and reboot system. Options available: Disabled, 2 minutes, 4 minutes, 6 minutes. Default setting is 2 minutes .
System Event Log	Press [Enter] to configure advanced items.

(Note1) This item is configurable when **FRB-2 Timer** is set to **Enabled**.

(Note2) This item is configurable when **OS Watchdog Timer** is set to **Enabled**.

Parameter	Description
View FRU Information	Press [Enter] to view the FRU information.
BMC network configuration	Press [Enter] to configure advanced items.
IPv6 BMC Network Configuration	Press [Enter] to configure advanced items.

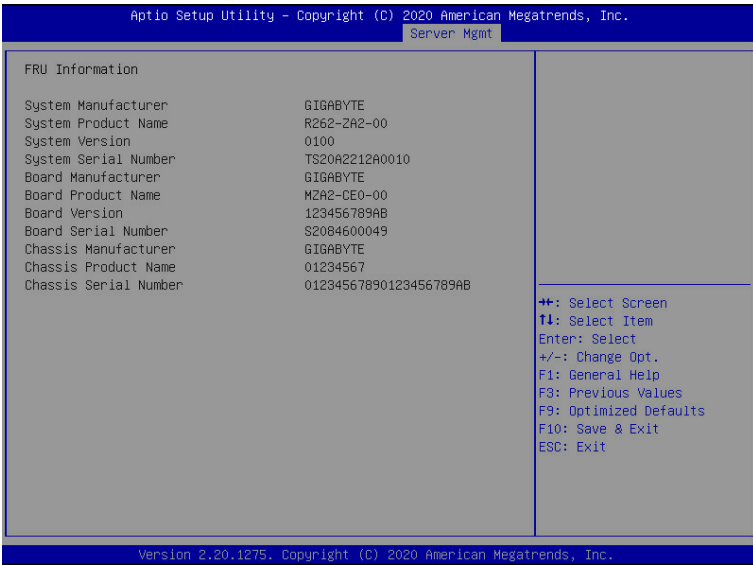
5-6-1 System Event Log



Parameter	Description
Enabling / Disabling Options	
SEL Components	Change this item to enable or disable all features of System Event Logging during boot. Options available: Enabled, Disabled. Default setting is Enabled .
Erasing Settings	
Erase SEL	Choose options for erasing SEL. Options available: No, Yes, On next reset, Yes, On every reset. Default setting is No .
When SEL is Full	Choose options for reactions to a full SEL. Options available: Do Nothing, Erase Immediately. Default setting is Do Nothing .
Custom EFI Logging Options	
Log EFI Status Codes	Enable/Disable the logging of EFI Status Codes (if not already converted to legacy). Options available: Disabled, Both, Error code, Progress code. Default setting is Error code .

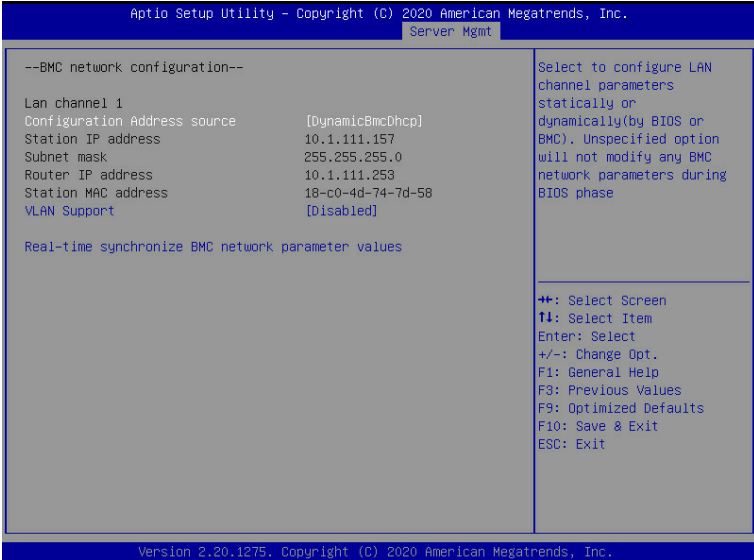
5-6-2 View FRU Information

The FRU page is a simple display page for basic system ID information, as well as System product information. Items on this window are non-configurable.



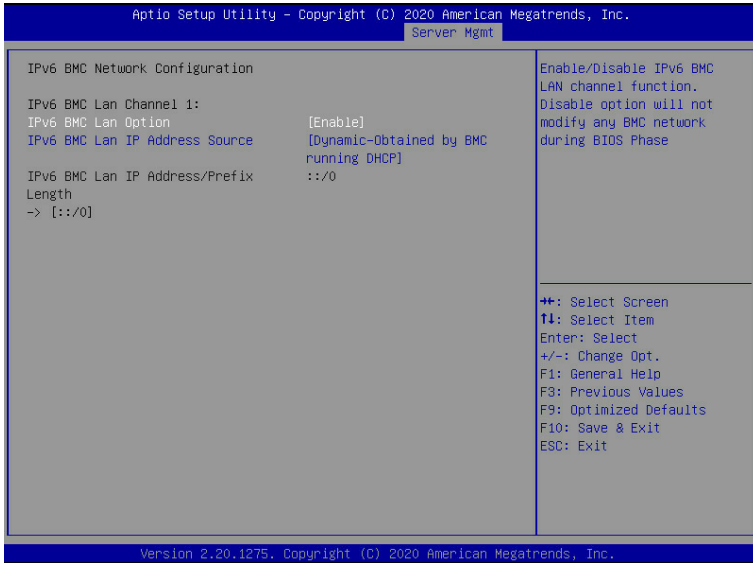
(Note) The model name will vary depends on the product you purchased

5-6-3 BMC Network Configuration



Parameter	Description
BMC network configuration	
Lan Channel 1	
Configuration Address source	Selects to configure LAN channel parameters statically or dynamically (DHCP). Do nothing option will not modify any BMC network parameters during BIOS phase. Options available: Unspecified, Static, DynamicBmcDhcp. Default setting is DynamicBmcDhcp .
Station IP address	Displays IP Address information.
Subnet mask	Displays Subnet Mask information. Please note that the IP address must be in three digitals, for example, 192.168.000.001.
Router IP address	Displays the Router IP Address information.
Station MAC address	Displays the MAC Address information.
VLAN Support	Set BMC to enable/disable VLAN support. Options available: Enabled, Disabled. Default setting is Disabled .
Real-time synchronize BMC network parameter values	Press [Enter] will set Address source(Static/DHCP) to BMC and then get Station IP address, Subnet mask and Router IP address from BMC.

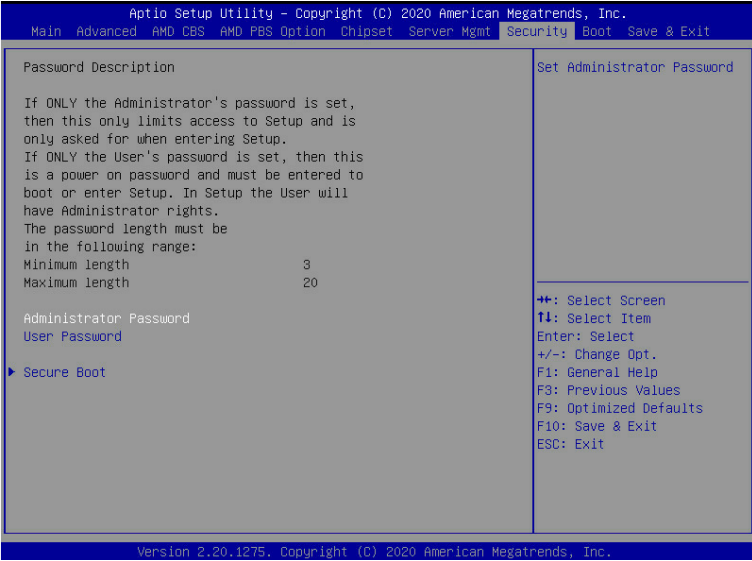
5-6-4 IPv6 BMC Network Configuration



Parameter	Description
IPv6 BMC network configuration	
IPv6 BMC Lan Channel 1	
IPv6 BMC Lan Option	Enable/Disable IPv6 BMC LAN channel function. When this item is disabled, the system will not modify any BMC network during BIOS phase. Options available: Unspecified, Disable, Enable. Default setting is Enable .
IPv6 BMC Lan IP Address Source	Selects to configure LAN channel parameters statically or dynamically (by BIOS or BMC). Options available: Unspecified, Static, Dynamic-Obtained by BMC running DHCP. Default setting is Enable Dynamic-Obtained by BMC running DHCP .
IPv6 BMC Lan IP Address/Prefix Length	Check if the IPv6 BMC LAN IP address matches those displayed on the screen.

5-7 Security Menu

The Security menu allows you to safeguard and protect the system from unauthorized use by setting up access passwords.



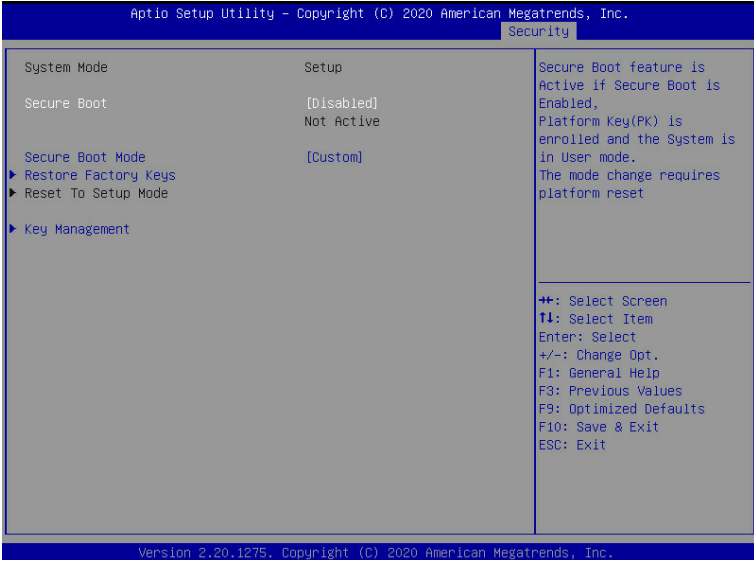
There are two types of passwords that you can set:

- Administrator Password
Entering this password will allow the user to access and change all settings in the Setup Utility.
- User Password
Entering this password will restrict a user's access to the Setup menus. To enable or disable this field, a Administrator Password must first be set. A user can only access and modify the System Time, System Date, and Set User Password fields.

Parameter	Description
Administrator Password	Press [Enter] to configure the administrator password.
User Password	Press [Enter] to configure the user password.
Secure Boot	Press [Enter] to configure advanced items.

5-7-1 Secure Boot

The Secure Boot submenu is applicable when your device is installed the Windows® 8 (or above) operating system.



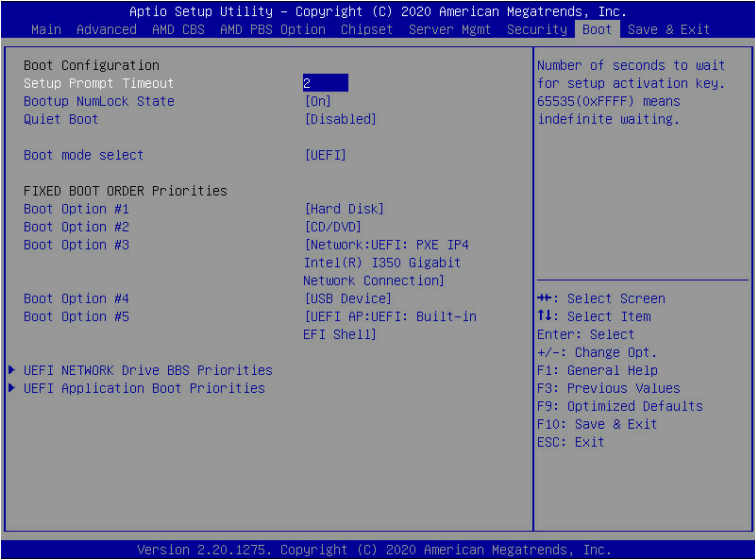
Parameter	Description
System Mode	Displays if the system is in User mode or Setup mode.
Secure Boot	Enable/ Disable the Secure Boot function. Options available: Enabled, Disabled. Default setting is Disabled .
Secure Boot Mode ^(Note)	Secure Boot requires all the applications that are running during the booting process to be pre-signed with valid digital certificates. This way, the system knows all files being loaded before Windows loads to the login screen have not been tampered with. When set to Standard, it will automatically load the Secure Boot keys form the BIOS databases. When set to Custom, you can customize the Secure Boot settings and manually load its keys from the BIOS database. Options available: Standard, Custom. Default setting is Standard .
Restore Factory Keys	Forces the system to user mode and installs factory default Secure Boot key database.

(Note) Advanced items prompt when this item is set to **Custom**.

Parameter	Description
Key Management	<p data-bbox="335 156 665 180">Press [Enter] to configure advanced items.</p> <p data-bbox="335 185 936 235">Please note that this item is configurable when Secure Boot Mode is set to Custom.</p> <ul style="list-style-type: none"> <li data-bbox="335 243 946 352">◆ Factory Key Provision <ul style="list-style-type: none"> <li data-bbox="367 266 946 321">– Allows to provision factory default Secure Boot keys when system is in Setup Mode. <li data-bbox="367 326 904 352">– Options available: Enabled, Disabled. Default setting is Disabled. <li data-bbox="335 357 946 431">◆ Restore Factory Keys <ul style="list-style-type: none"> <li data-bbox="367 381 925 404">– Installs all factory default keys. It will force the system in User Mode. <li data-bbox="367 409 606 431">– Options available: Yes, No. <li data-bbox="335 435 946 517">◆ Enroll Efi Image <ul style="list-style-type: none"> <li data-bbox="367 459 899 517">– Press [Enter] to enroll SHA256 hash of the binary into Authorized Signature Database (db). <li data-bbox="335 522 946 572">◆ Restore DB defaults <ul style="list-style-type: none"> <li data-bbox="367 545 702 572">– Restore DB variable to factory defaults. <li data-bbox="335 577 946 627">◆ Secure Boot variable <ul style="list-style-type: none"> <li data-bbox="367 600 893 627">– Displays the current status of the variables used for secure boot. <li data-bbox="335 631 946 744">◆ Platform Key (PK) <ul style="list-style-type: none"> <li data-bbox="367 655 803 682">– Displays the current status of the Platform Key (PK). <li data-bbox="367 686 680 713">– Press [Enter] to configure a new PK. <li data-bbox="367 718 601 744">– Options available: Update. <li data-bbox="335 749 946 885">◆ Key Exchange Keys (KEK) <ul style="list-style-type: none"> <li data-bbox="367 773 941 854">– Displays the current status of the Key Exchange Key Database (KEK). <li data-bbox="367 804 904 854">– Press [Enter] to configure a new KEK or load additional KEK from storage devices. <li data-bbox="367 859 670 885">– Options available: Update, Append. <li data-bbox="335 890 946 1027">◆ Authorized Signatures (DB) <ul style="list-style-type: none"> <li data-bbox="367 914 904 937">– Displays the current status of the Authorized Signature Database. <li data-bbox="367 942 946 992">– Press [Enter] to configure a new DB or load additional DB from storage devices. <li data-bbox="367 997 670 1023">– Options available: Update, Append. <li data-bbox="335 1031 946 1168">◆ Forbidden Signatures (DBX) <ul style="list-style-type: none"> <li data-bbox="367 1055 899 1078">– Displays the current status of the Forbidden Signature Database. <li data-bbox="367 1083 893 1133">– Press [Enter] to configure a new dbx or load additional dbx from storage devices. <li data-bbox="367 1138 670 1165">– Options available: Update, Append. <li data-bbox="335 1172 946 1309">◆ Authorized TimeStamps (DBT) <ul style="list-style-type: none"> <li data-bbox="367 1196 925 1219">– Displays the current status of the Authorized TimeStamps Database. <li data-bbox="367 1224 904 1274">– Press [Enter] to configure a new DBT or load additional DBT from storage devices. <li data-bbox="367 1279 670 1306">– Options available: Update, Append. <li data-bbox="335 1313 946 1442">◆ OsRecovery Signatures <ul style="list-style-type: none"> <li data-bbox="367 1337 920 1361">– Displays the current status of the OsRecovery Signature Database. <li data-bbox="367 1365 888 1415">– Press [Enter] to configure a new OsRecovery Signature or load additional OsRecovery Signature from storage devices. <li data-bbox="367 1420 670 1447">– Options available: Update, Append.

5-8 Boot Menu

The Boot menu allows you to set the drive priority during system boot-up. BIOS setup will display an error message if the legacy drive(s) specified is not bootable.

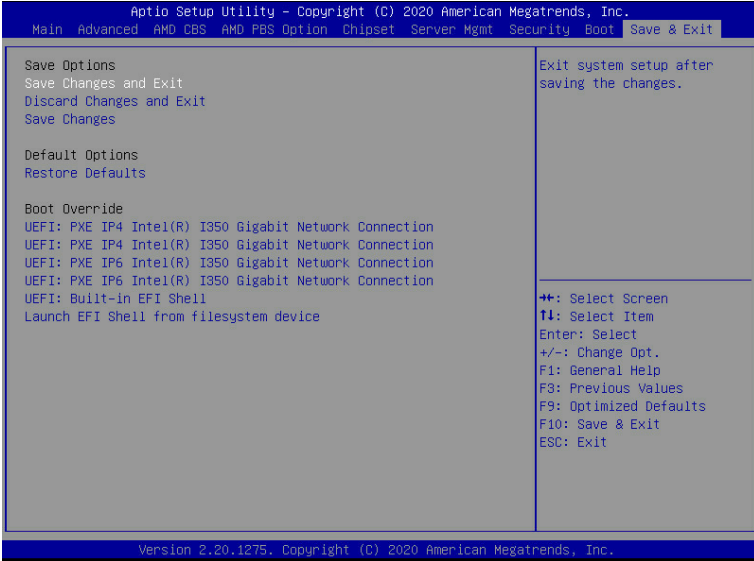


Parameter	Description
Boot Configuration	
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting. Press the numeric keys to input the desired values.
Bootup NumLock State	Enable/Disable the Bootup NumLock function. Options available: On, Off. Default setting is Off .
Quiet Boot	Enable/Disable showing the logo during POST. Options available: Enabled, Disabled. Default setting is Enabled .
Boot mode select	Selects the boot mode. Options available: LEGACY, UEFI. Default setting is UEFI .

Parameter	Description
FIXED BOOT ORDER Priorities	
Boot Option #1 / #2 / #3 / #4 / #5	<p data-bbox="402 200 948 283">Press [Enter] to configure the boot order priority. By default, the server searches for boot devices in the following sequence:</p> <ol data-bbox="440 288 948 426" style="list-style-type: none"> <li data-bbox="440 288 948 312">1. Hard drive. <li data-bbox="440 316 948 340">2. CD-COM/DVD drive. <li data-bbox="440 344 948 368">3. USB device. <li data-bbox="440 373 948 396">4. Network. <li data-bbox="440 401 948 424">5. UEFI.
UEFI Network Drive BBS Priorities	Press [Enter] to configure the boot priority.
UEFI Application Boot Priorities	Press [Enter] to configure the boot priority.

5-9 Save & Exit Menu

The Save & Exit menu displays the various options to quit from the BIOS setup. Highlight any of the exit options then press <Enter>.



Parameter	Description
Save Options	
Save Changes and Exit	Saves changes made and closes the BIOS setup. Options available: Yes, No.
Discard Changes and Exit	Discards changes made and exits the BIOS setup. Options available: Yes, No.
Save Changes	Saves changes done so far to any of the setup options. Options available: Yes, No.
Default Options	
Restore Defaults	Loads the default settings for all BIOS setup parameters. Setup Defaults are quite demanding in terms of resources consumption. If you are using low-speed memory chips or other kinds of low-performance components and you choose to load these settings, the system might not function properly. Options available: Yes, No.
Boot Override	Press [Enter] to configure the device as the boot-up drive.
Launch EFI Shell from filesystem device	Attempts to Launch EFI Shell application (Shell.efi) from one of the available file system devices.

5-10 ABL POST Codes

5-10-1 StartProcessorTestPoints

Entry used for range testing for @b Processor related TPs	0xE000
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5-10-2 Memory test points

Memory structure initialization (Public interface)	0xE001
SPD Data processing (Public interface)	0xE002
Memory configuration (Public interface) Phase 1	0xE003
DRAM initialization	0xE004
ProcMemSPDChecking	0xE005
ProcMemModeChecking	0xE006
Speed and TCL configuration	0xE007
ProcMemSpdTiming	0xE008
ProcMemDramMapping	0xE009
ProcMemPlatformSpecificConfig	0xE00A
ProcMemPhyCompensation	0xE00B
ProcMemStartDcts	0xE00C
ProcMemBeforeDramInit (Public interface)	0xE00D
ProcMemPhyFenceTraining	0xE00E
ProcMemSynchronizeDcts	0xE00F
ProcMemSystemMemoryMapping	0xE010
ProcMemMtrrConfiguration	0xE011
ProcMemDramTraining	0xE012
ProcMemBeforeAnyTraining(Public interface)	0xE013

5-10-3 PMU Test Points

ABL Mem - PMU - Before PMU Firmware load	0xE014
ABL Mem - PMU - After PMU Firmware load	0xE015
ABL Mem - PMU Populate SRAM Timing	0xE016
ABL Mem - PMU Populate SRAM Config	0xE017
ABL Mem - PMU Write SRAM Msg Block	0xE018
ABL Mem - Wait for Phy Cal Complete	0xE019
ABL Mem - Phy Cal Complete	0xE01A
ABL Mem - PMU Start	0xE01B
ABL Mem - PMU Started	0xE01C
ABL Mem - PMU Waiting for Complete	0xE01D
ABL Mem - PMU Stage Dec Init	0xE01E
ABL Mem - PMU Stage Training Wr Lvl	0xE01F
ABL Mem - PMU Stage Training Rx En	0xE020
ABL Mem - PMU Stage Training Rd Dqs	0xE021
ABL Mem - PMU Stage Training Rd 2D	0xE022

ABL Mem - PMU Stage Training Wr 2D	0xE023
ABL Mem - PMU Queue Empty	0xE024
ABL Mem - PMU US message Start	0xE025
ABL Mem - PMU US message End	0xE026
ABL Mem - PMU Complete	0xE027
ABL Mem - PMU - After PMU Training	0xE028
ABL Mem - PMU - Before Disable PMU	0xE029

5-10-4 Original Post Code

ProcMemTransmitDqsTraining	0xE02A
ABL Mem - Start write sweep	0xE02B
ABL Mem - Set Transmit DQ delay	0xE02C
ABL Mem - Write test pattern	0xE02D
ABL Mem - Read Test pattern	0xE02E
ABL Mem - Compare Test pattern	0xE02F
ABL Mem - Update results	0xE030
ABL Mem - Start Find passing window	0xE031
ABL Mem - ProcMemMaxRdLatencyTraining	0xE032
ABL Mem - Start sweep	0xE033
ABL Mem - Set delay	0xE034
ABL Mem - Write test pattern	0xE035
ABL Mem - Read Test pattern	0xE036
ABL Mem - Compare Test pattern	0xE037
ABL Mem - Online Spare init	0xE038
ABL Mem - Chip select Interleave Init	0xE039
ABL Mem - Node Interleave Init	0xE03A
ABL Mem - Channel Interleave Init	0xE03B
ABL Mem - ECC initialization	0xE03C
ABL Mem - Platform Specific Init	0xE03D
ABL Mem - Before callout for "AgesaReadSpd"	0xE03E
ABL Mem - After callout for "AgesaReadSpd"	0xE03F
ABL Mem - Before optional callout "AgesaHookBeforeDramInit"	0xE040
ABL Mem - After optional callout "AgesaHookBeforeDramInit"	0xE041
ABL Mem - Before optional callout "AgesaHookBeforeDQSTraining"	0xE042
ABL Mem - After optional callout "AgesaHookBeforeDQSTraining"	0xE043
ABL Mem - Before optional callout "AgesaHookBeforeDramInit"	0xE044
ABL Mem - After optional callout "AgesaHookBeforeDramInit"	0xE045
ABL Mem - After MemDataInit	0xE046
ABL Mem - Before InitializeMCT	0xE047
ABL Mem - Before LV DDR3	0xE048
ABL Mem - Before InitMCT	0xE049

ABL Mem - Before OtherTiming	0xE04A
ABL Mem - Before UMAMemTyping	0xE04B
ABL Mem - Before SetDqsEccTmgs	0xE04C
ABL Mem - Before MemClr	0xE04D
ABL Mem - Before On DIMM Thermal	0xE04E
ABL Mem - Before DMI	0xE04F
ABL MEM - End of phase 3 memory code	0xE050

5-10-5 CPU test points

Entry point CPU init after training	0xE051
Exit point CPU init after training	0xE052
Entry point CPU APOB CCX map init	0xE053
Exit point CPU APOB CCX map init	0xE054
Entry point CPU Optimized boot init	0xE055
Exit point CPU Optimized boot init	0xE056
Entry point CPU APOB EDC info init	0xE057
Exit point CPU APOB EDC info init	0xE058

5-10-6 Topology test points

ProcTopologyEntry	0xE071
ProcTopologyDone	0xE07C

5-10-7 Extended memory test point

ProcMemSendMRS2	0xE080
Sedding MRS3	0xE081
Sending MRS1	0xE082
Sending MRS0	0xE083
Continuous Pattern Read	0xE084
Continuous Pattern Write	0xE085
Mem: 2d RdDqs Training begin	0xE086
Mem: Before optional callout to platform BIOS to change External Vref during 2d Training	0xE087
Mem: After optional callout to platform BIOS to change External Vref during 2d Training	0xE088
Configure DCT For General use begin	0xE089
Configure DCT For training begin	0xE08A
Configure DCT For Non-Explicit	0xE08B
Configure to Sync channels	0xE08C
Allocate C6 Storage	0xE08D
Before LV DDR4	0xE08E
Before LV DDR3	0xE08F

5-10-8 Gnb Earlier init

TP0x90	0xE090
GNB earlier interface	0xE091
GNB internal debug code	0xE092
GNB internal debug code	0xE093
GNB internal debug code	0xE094
GNB internal debug code	0xE095
GNB internal debug code	0xE096
GNB internal debug code	0xE097
GNB internal debug code	0xE098
GNB internal debug code	0xE099
GNB internal debug code	0xE09A
GNB internal debug code	0xE09B
GNB internal debug code	0xE09C
GNB internal debug code	0xE09D
GNB internal debug code	0xE09E
GNB internal debug code	0xE09F
TP0xA0	0xE0A0
GNB internal debug code	0xE0A1
GNB internal debug code	0xE0A2
GNB internal debug code	0xE0A3
GNB internal debug code	0xE0A4
GNB internal debug code	0xE0A5
GNB internal debug code	0xE0A6
GNB internal debug code	0xE0A7
GNB internal debug code	0xE0A8
GNB internal debug code	0xE0A9
GNB internal debug code	0xE0AA
GNB internal debug code	0xE0AB
GNB internal debug code	0xE0AC
GNB internal debug code	0xE0AD
GNB internal debug code	0xE0AE
GNB internal debug code	0xE0AF
Abl1Begin	0xE0B0
ABL 1 Initialization	0xE0B1
ABL 1 DF Early	0xE0B2
ABL 1 DF Pre Training	0xE0B3
ABL 1 Debug Synchronization	0xE0B4
ABL 1 Error Detected	0xE0B5
ABL 1 Global memory error detected	0xE0B6
ABL 1 End	0xE0B7

ABL 2 Begin	0xE0B8
ABL 2 Initialization	0xE0B9
ABL 2 After Training	0xE0BA
ABL 2 Debug Synchronization	0xE0BB
ABL 2 Error detected	0xE0BC
ABL 2 Global memory error detected	0xE0BD
ABL 2 End	0xE0BE
ABL 3 Begin	0xE0BF
ABL 3 Initialization	0xE0C0
ABL 3 GMI/xGMI Initialization Stage 1	0xB1C0
ABL 3 GMI/xGMI Initialization Stage 1 Warning	0xF1C0
ABL 3 GMI/xGMI Initialization Stage 2 Error	0xE2C0
ABL 3 GMI/xGMI Initialization Stage 2	0xB2C0
ABL 3 GMI/xGMI Initialization Stage 2 Warning	0xF2C0
ABL 3 GMI/xGMI Initialization Stage 2 Error	0xE3C0
ABL 3 GMI/xGMI Initialization Stage 3	0xB3C0
ABL 3 GMI/xGMI Initialization Stage 3 Warning	0xF3C0
ABL 3 GMI/xGMI Initialization Stage 3 Error	0xE4C0
ABL 3 GMI/xGMI Initialization Stage 4	0xB4C0
ABL 3 GMI/xGMI Initialization Stage 4 Warning	0xF4C0
ABL 3 GMI/xGMI Initialization Stage 4 Error	0xE5C0
ABL 3 GMI/xGMI Initialization Stage 5	0xB5C0
ABL 3 GMI/xGMI Initialization Stage 5 Warning	0xF5C0
ABL 3 GMI/xGMI Initialization Stage 5 Error	0xE6C0
ABL 3 GMI/xGMI Initialization Stage 6	0xB6C0
ABL 3 GMI/xGMI Initialization Stage 6 Warning	0xF6C0
ABL 3 GMI/xGMI Initialization Stage 6 Error	0xE7C0
ABL 3 GMI/xGMI Initialization Stage 7	0xE8C0
ABL 3 GMI/xGMI Initialization Stage 8	0xE9C0
ABL 3 GMI/xGMI Initialization Stage 9	0xF9C0
ABL 3 GMI/xGMI Initialization Stage 9 Error	0xEAC0
ABL 3 GMI/xGMI Initialization Stage 10	0xFAC0
ABL 3 GMI/xGMI Initialization Stage 10 Error	0xE0C1
Abi3ProgramUmcKeys	0xE0C2
ABL 3 DF Final Initialization	0xE0C3
ABL 3 Execute Synchronization Function	0xE0C4
ABL 3 Debug Synchronization Function	0xE0C5
ABL 3 Error Detected	0xE0C6
ABL 3 Global memory error detected	0xE0C7
ABL 4 Initialization - cold boot	0xE0C8
ABL 4 Memory test - cold boot	0xE0C9

ABL 4 APOB Initialization - cold boot	0xE0CA
ABL 4 Finalize memory settings - cold boot	0xE0CB
ABL 4 CPU Initialize Optimized Boot - cold boot	0xE0CC
ABL 4 Gmi Pcie Training - cold boot	0xE0CD
ABL 4 Cold boot End	0xE0CE
ABL 4 Initialization - Resume boot	0xE0CF
ABL 4 Resume End	0xE0D0
ABL 4 End Cold/Resume boot	0xE0D1
ABL 2 memory initialization	0xE0D2
ABL 3 memory initialization	0xE0D3
ABL 3 End	0xE0D4
ABL 1 Enter Memory Flow	0xE0D5
Memory flow memory clock synchronization	0xE0D6
IfAmdReadEventLogEntry	0xE0D7
Exiting from AmdReadEventLog	0xE0D8
Entry to AmdGetApicId	0xE0D9
Exiting from AmdGetApicId	0xE0DA
Entry to AmdGetPciAddress	0xE0DB
Exiting from AmdGetPciAddress	0xE0DC
Entry to AmdIdentifyCore	0xE0DD
TExiting from AmdIdentifyCore	0xE0DE
After IDS calls out to run code on an AP	0xE0DF
After IDS calls out to run code on an AP	0xE0E0
Before IDS calls out to get IDS data	0xE0E1
After IDS calls out to get IDS data	0xE0E2
Before the heap manager calls out to allocate a buffer	0xE0E3
After the heap manager calls out to allocate a buffer	0xE0E4
Before the heap manager calls out to deallocate a buffer	0xE0E5
After the heap manager calls out to deallocate a buffer	0xE0E6
Before the heap manager calls out to locate a buffer	0xE0E7
After the heap manager calls out to locate a buffer	0xE0E8
Memory flow P-State synchronization	0xE0E9
After the BSP calls out to run code on an AP	0xE0EA
Before the BSP calls out to run code on an AP	0xE0EB
After the BSP calls out to run code on an AP	0xE0EC
Before the S3 save code calls out to allocate a buffer	0xE0ED
After the S3 save code calls out to allocate a buffer	0xE0EE
Before the memory S3 save code calls out to allocate a buffer	0xE0EF
After the memory S3 save code calls out to allocate a buffer	0xE0F0
Before the memory code calls out to locate a buffer	0xE0F1
After the memory code calls out to locate a buffer	0xE0F2

Before the memory code calls out to locate a buffer	0xE0F3
After the memory code calls out to locate a buffer	0xE0F4
Before the memory code calls out to locate a buffer	0xE0F5
After the memory code calls out to locate a buffer	0xE0F6
Before the memory code calls out to locate a buffer	0xE0F7
After the memory code calls out to locate a buffer	0xE0F8
Ready to boot event	

5-10-9 PMU test points

Failed PMU training	0xE0F9
End of phase 1 memory code	0xE0FA
End of phase 2 memory code	0xE0FB

5-10-10 ABL0 test points

Abl0Begin	0xE0FC
ABL 0 End	0xE0FD

5-10-11 ABL5 test points

ABL 5 End	0xE100
sume boot	0xE101
ABL 6 End	0xE102
ABL 6 Initialization	0xE103
End of phase 1b memory code	0xE104
ABL 1b memory initialization	0xE105
ABL 6 Global memroy error detected	0xE106
ABL 1b Debug Synchronization Function	0xE107
ABL 4b Debug Synchronization Function	0xE108
Ab1bBegin	0xE109
Ab4bBegin	0xE10A
BSP encountered HMAC fail on APOB Header	0xE10B
ABL Error General ASSERT	0xE2A0
Unknown Error	0xE2A1
ABL Error Log Inig Error	0xE2A2
ABL Error for On DIMM thermal Heap allocation error	0xE2A3
ABL Error for memory test error	0xE2A4
ABL Error while executing memory test error	0xE2A5
ABL Error DDR Post Package Repair Mem Auto Heap Alloc error	0xE2A6
ABL Error for DDR Post Package repair Apob Heap Alloc error	0xE2A7
ABL Error for DDR Post Package Repair No PPR Table Heap Alloc error	0xE2A8
ABL Error for Ecc Mem Auto Aloc Error error	0xE2A9
ABL Error for Soc Scan Heap Alloc error	0xE2AB

ABL Error for Soc Scan No Die error	0xE2AC
ABL Error for Nb Tech Heap Alloc error	0xE2AD
ABL Error for No Nb Constructor error	0xE2AE
ABL Error for No Tech Constructor error	0xE2AE
ABL Error for ABL1b Auto Allocation error	0xE2B0
ABL Error for ABL1b No NB Constructor error	0xE2B1
ABL Error for ABL2 No Nb Constructor error	0xE2B2
ABL Error for ABL3 Auto Allocation error	0xE2B3
ABL Error for ABL3 No Nb Constructor error	0xE2B4
ABL Error for ABL1b General error	0xE2B5
ABL Error for ABL2 General error	0xE2B6
ABL Error for ABL3 General error	0xE2B7
ABL Error for Get Target Speed error	0xE2B8
ABL Error for Flow P1 Family Support error	0xE2B9
ABL Error for No Valid Ddr4 Dimms error	0xE2BA
ABL Error for No Dimm Present error	0xE2BB
ABL Error for Flow P2 Family Supprot error	0xE2BC
ABL Error for Heap Deallocation for PMU Sram Msg Block error	0xE2BD
ABL Error for DDR Recovery error	0xE2BE
ABL Error for RRW Test error	0xE2BF
ABL Error for On Die Thermal error	0xE2C1
ABL Error for Heap Allocation For Dct Struct Amd Ch Def structure error	0xE2C2
ABL Error for Heap Allocation for PMU SRAM Msg block error	0xE2C3
ABL Error for Heap Phy PLL lock Flure error	0xE2C4
ABL Error for Pmu Training error	0xE2C5
ABL Error for Failure to Load or Verify PMU FW error	0xE2C6
ABL Error for Allocate for PMU SRAM Msg Block No Init error	0xE2C7
ABL Error for Failure BIOS PMU FW Mismatch AGESA PMU FW version error	0xE2C8
ABL Error for Deallocate for PMU SRAM Msg Block error	0xE2CA
ABL Error for Module Type Mismatch RDIMM error	0xE2CB
ABL Error for Module type Mismatch LRDIMM error	0xE2CC
ABL Error for MEm Auto NVDIM error	0xE2CD
ABL Error for Unknowm Responce error	0xE2CE
ABL Error for Over Clock Error RRW Test Results Error	0xE2CF
ABL Error for Over Clock Error PMU Training Error	0xE2D0
ABL Error for ABL1 General Error	0xE2D1
ABL Error for ABL2 General Error	0xE2D2
ABL Error for ABL3 General Error	0xE2D3
ABL Error for ABL4 General Error	0xE2D4

ABL Error over clock Mem Init Error	0xE2D5
ABL Error over clock Mem Other Error	0xE2D6
ABL Error for ABL6 General Error	0xE2D7
ABL Error Event Log Error	0xE2D8
ABL Error FATAL ABL1 Log Error	0xE2D9
ABL Error FATAL ABL2 Log Error	0xE2DA
ABL Error FATAL ABL3 Log Error	0xE2DB
ABL Error FATAL ABL4 Log Error	0xE2DC
ABL Error Slave Sync function execution Error	0xE2DD
ABL Error Slave Sync communicaton with data set to master Error	0xE2DE
ABL Error Slave broadcast communication from master to slave Error	0xE2DF
ABL Error FATAL ABL6 Log Error	0xE2E0
ABL Error Slave Offline Error	0xE2E1
ABL Error Slave Informs Master Error Info Error	0xE2E2
ABL Error Error Heap Locate for PMU SRAM Msg Block Error	0xE2E3
ABL Error ABL2 Auto Error	0xE2E4
ABL Error Flow P3 Family support Error	0xE2E5
ABL Error Abl 4 Gen Error	0xE2EB
ABL Error MBIST Heap Allocation Error	0xE2EC
ABL Error MBIST Results Error	0xE2EE
ABL Error NO Dimm Smcus Info Error	0xE2EE
ABL Error Por Max Freq Table Error	0xE2EF
ABL Error Unsupproted DIMM Config Error	0xE2F0
ABL Error No Ps Table Error	0xE2F1
ABL Error Cad Bus Timing Not Found Error	0xE2F2
ABL Error Data Bus Timing Not Found Error	0xE2F3
ABL Error LrDIMM IBT Not Found Error	0xE2F4
ABL Error Unsuppote Dimm Config Max Freq Error Error	0xE2F5
ABL Error Mr0 Not Found Error	0xE2F6
ABL Error Obt Pattern Not found Error	0xE2F7
ABL Error Rc10 Op Speed Not FOUNd Error	0xE2F8
ABL Error Rc2 Ibt Not Found Error	0xE2F9
ABL Error Rtt Not Found Error	0xE2FA
ABL Error Checksum ReStrt Results Error	0xE2FB
ABL Error No Chipselect Results Error	0xE2FC
ABL Error No Common Cas Latency Results Error	0xE2FD
ABL Error Cas Latecncy exceeds Taa Max Error	0xE2FE
ABL Error Nvdimm Arm Mismatch Power Policy Error	0xE2FF
ABL Error Nvdimm Arm Mismatch Power Source Error	0xE300
ABL Error ABL 1 Mem Init Error	0xE301

ABL Error ABL 2 Mem Init Error	0xE302
ABL Error ABL 4 Mem Init Error	0xE303
ABL Error ABL 6 Mem Init Error	0xE304
ABL Error ABL 1 error repor Error	0xE305
ABL Error ABL 2 error repor Error	0xE306
ABL Error ABL 3 error repor Error	0xE307
ABL Error ABL 4 error repor Error	0xE308
ABL Error ABL 6 error repor Error	0xE30A
ABL Error message slave sync function execution Error	0xE30B
ABL Error slave offline Error	0xE30C
ABL Error Sync Master Error	0xE30D
ABL Error Slave Informs Master Info Message Error	0xE30E
ABL Error General Assert Error	0xE30F
ABL Error No Dimms On Any Channel in sysem	0xE310
ABL Alert PMU Major Message captured	0xE311
ABL Alert PMU REsults Rx Timing captured	0xE312
ABL Alert PMU REsults Tx Timing captured	0xE313
ABL Alert PMU REsults Rx Vref captured	0xE314
ABL Alert PMU REsults Tx Vref captured	0xE315
EndAgesas	0xEFFF

5-11 Agesa POST Codes

5-11-1 Universal Post Code

Universal ACPI entry	0xA001
Universal ACPI exit	0xA002
Universal ACPI abort	0xA003
Universal SMBIOS entry	0xA004
Universal SMBIOS exit	0xA005
Universal SMBIOS abort	0xA006

5-11-2 [0xA1XX] For CZ only memory Postcodes

Memory structure initialization (Public interface)	0xA101
SPD Data processing (Public interface)	0xA102
Memory configuration (Public interface)	0xA103
DRAM initialization	0xA104
TpProcMemSPDChecking	0xA105
TpProcMemModeChecking	0xA106
Speed and TCL configuration	0xA107
TpProcMemSpdTiming	0xA108
TpProcMemDramMapping	0xA109
TpProcMemPlatformSpecificConfig	0xA10A
TPProcMemPhyCompensation	0xA10B
TpProcMemStartDcts	0xA10C
(Public interface)	0xA10D
TpProcMemPhyFenceTraining	0xA10E
TpProcMemSynchronizeDcts	0xA10F
TpProcMemSystemMemoryMapping	0xA110
TpProcMemMtrrConfiguration	0xA111
TpProcMemDramTraining	0xA112
(Public interface)	0xA113
TpProcMemWriteLevelizationTraining	0xA114
Below 800Mhz first pass start	0xA115
Above 800Mhz second pass start	0xA116
Target DIMM configured	0xA117
Prepare DIMMS for WL	0xA118
Configure DIMMS for WL	0xA119
TpProcMemReceiverEnableTraining	0xA11A
Start sweep loop	0xA11B
Set receiver Delay	0xA11C
Write test pattern	0xA11D
Read test pattern	0xA11E
Compare test pattern	0xA11F

Calculate MaxRdLatency per channel	0xA120
TpProcMemReceiveDqsTraining	0xA121
Set Write Data delay	0xA122
Write test pattern	0xA123
Start read sweep	0xA124
Set Receive DQS delay	0xA125
Read Test pattern	0xA126
Compare Test pattern	0xA127
Update results	0xA128
Start Find passing window	0xA129
TpProcMemTransmitDqsTraining	0xA12A
Start write sweep	0xA12B
Set Transmit DQ delay	0xA12C
Write test pattern	0xA12D
Read Test pattern	0xA12E
Compare Test pattern	0xA12F
Update results	0xA130
Start Find passing window	0xA131
TpProcMemMaxRdLatencyTraining	0xA132
Start sweep	0xA133
Set delay	0xA134
Write test pattern	0xA135
Read Test pattern	0xA136
Compare Test pattern	0xA137
Online Spare init	0xA138
Bank Interleave Init	0xA139
Node Interleave Init	0xA13A
Channel Interleave Init	0xA13B
ECC initialization	0xA13C
Platform Specific Init	0xA13D
Before callout for "AgesaReadSpd"	0xA13E
After callout for "AgesaReadSpd"	0xA13F
Before optional callout "AgesaHookBeforeDramInit"	0xA140
After optional callout "AgesaHookBeforeDramInit"	0xA141
Before optional callout "AgesaHookBeforeDQSTraining"	0xA142
After optional callout "AgesaHookBeforeDQSTraining"	0xA143
Before optional callout "AgesaHookBeforeDramInit"	0xA144
After optional callout "AgesaHookBeforeDramInit"	0xA145
After MemDataInit	0xA146
Before InitializeMCT	0xA147
Before LV DDR3	0xA148

Before InitMCT	0xA149
Before OtherTiming	0xA14A
Before UMAMemTyping	0xA14B
Before SetDqsEccTmgs	0xA14C
Before MemClr	0xA14D
Before On DIMM Thermal	0xA14E
Before DMI	0xA14F
End of memory code	0xA150
Entry point S3Init	0xA151
Sending MRS2	0xA180
Sedding MRS3	0xA181
Sending MRS1	0xA182
Sending MRS0	0xA183
Continuous Pattern Read	0xA184
Continuous Pattern Write	0xA185
Mem: 2d RdDqs Training begin	0xA186
Mem: Before optional callout to platform BIOS to change External Vref during 2d Training	0xA187
Mem: After optional callout to platform BIOS to change External Vref during 2d Training	0xA188
Configure DCT For General use begin	0xA189
Configure DCT For training begin	0xA18A
Configure DCT For Non-Explicit	0xA18B
Configure to Sync channels	0xA18C
Allocate C6 Storage	0xA18D
Before LV DDR4	0xA18E
// BR CPU	
BR before AP launch	0xA190
Install AP launched PPI	0xA191
BR after AP launch	0xA192
Before CPU PM	0xA193
Enable IO Cstate	0xA194
Enable C6	0xA195
Install CCX PEI complete PPI	0xA196
BR CPU memory done call back entry	0xA197
Before APM weights	0xA198
After APM weights	0xA199
BR CPU memory done call back end	0xA19A
BR Init Mid entry	0xA19B
BR enable APM	0xA19C
BR Init Mid install protocol	0xA19D

BR Init Mid end	0xA19E
BR Init Late entry	0xA19F
BR Init Late install protocol	0xA1A0
BR Init Late end	0xA1A1
BR DXE install complete protocol	0xA1A2
UNB install complete PPI	0xA1A3
UNB AfterApLaunch callback entry	0xA1A4
UNB AfterApLaunch callback end	0xA1A5

5-11-3 S3 Interface Post Code

Before the S3 save code calls out to allocate a buffer	0xA1EC
After the S3 save code calls out to allocate a buffer	0xA1ED
Before the memory S3 save code calls out to allocate a buffer	0xA1EE
After the memory S3 save code calls out to allocate a buffer	0xA1EF
Before the memory code calls out to locate a buffer	0xA1F0
After the memory code calls out to locate a buffer	0xA1F1
Before the memory code calls out to locate a buffer	0xA1F2
After the memory code calls out to locate a buffer	0xA1F3
Before the memory code calls out to locate a buffer	0xA1F4
After the memory code calls out to locate a buffer	0xA1F5
Before the memory code calls out to locate a buffer	0xA1F6
After the memory code calls out to locate a buffer	0xA1F7

5-11-4 PMU Post Code

Failed PMU training	0xA1F9
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5-11-5 [0xA5XX] assigned for AGESA PSP Module

// PSP V1 Modules	
PspPeiV1 entry	0xA501
PspPeiV1 exit	0xA502
MemoryDiscoveredPpiCallback entry	0xA503
MemoryDiscoveredPpiCallback exit	0xA504
PspDxeV1 entry	0xA507
PspDxeV1 exit	0xA508
PspDxeV1 PspPciEnumerationCompleteCallBack entry	0xA50A
PspDxeV1 PspPciEnumerationCompleteCallBack exit	0xA50B
PspDxeV1 ready to boot entry	0xA50C
PspDxeV1 ready to boot exit	0xA50D
PspSmmV1 entry	0xA50E
PspSmmV1 exit	0xA50F
PspSmmV1 SwSmiCallBack entry, build the S3 save area for resume	0xA510

PspSmmV1 SwSmiCallBack exit, build the S3 save area for resume	0xA511
PspSmmV1 BspSmmResumeVector entry	0xA512
PspSmmV1 BspSmmResumeVector exit	0xA513
PspSmmV1 ApSmmResumeVector entry	0xA514
PspSmmV1 ApSmmResumeVector exit	0xA515
PspP2CmboxV1 entry	0xA516
PspP2CmboxV1 exit	0xA517
// PSP V2 Modules	
PspPeiV2 entry	0xA521
PspPeiV2 exit	0xA522
PspDxeV2 entry	0xA523
PspDxeV2 exit	0xA524
PspDxeV2 PspMpServiceCallBack entry	0xA525
PspDxeV2 PspMpServiceCallBack exit	0xA526
PspDxeV2 FlashAccCallBack entry	0xA527
PspDxeV2 FlashAccCallBack exit	0xA528
PspDxeV2 ready to boot entry	0xA529
PspDxeV2 ready to boot exit	0xA52A
PspDxeV2 exit boot service entry	0xA52B
PspDxeV2 exit boot service exit	0xA52C
PspSmmV2 entry	0xA52D
PspSmmV2 exit	0xA52E
PspSmmV2 SwSmiCallBack entry, build the S3 save area for resume	0xA52F
PspSmmV2 SwSmiCallBack exit, build the S3 save area for resume	0xA530
PspSmmV2 BspSmmResumeVector entry	0xA531
PspSmmV2 BspSmmResumeVector exit	0xA532
PspSmmV2 ApSmmResumeVector entry	0xA533
PspSmmV2 ApSmmResumeVector exit	0xA534
PspP2CmboxV2 entry	0xA535
PspP2CmboxV2 exit	0xA536
TpPspRecoverApcbFail	0xA537
// PSP fTpm modules	
PspfTpmPei entry	0xA540
PspfTpmPei exit	0xA541
PspfTpmPei memory callback entry	0xA542
PspfTpmPei memory callback exit	0xA543
PspfTpmDxe entry	0xA544
PspfTpmDxe exit	0xA545
// P2C mailbox Handling [0xA59X]	
PspP2Cmbox Command SpiGetAttrib Handling entry	0xA591

PspP2Cmbox Command SpiSetAttrib Handling entry	0xA592
PspP2Cmbox Command SpiGetBlockSize Handling entry	0xA593
PspP2Cmbox Command SpiReadFV Handling entry	0xA594
PspP2Cmbox Command SpiWriteFV Handling entry	0xA595
PspP2Cmbox Command SpiEraseFV Handling entry	0xA596
PspP2Cmbox Command Handling exit	0xA59E
PspP2Cmbox Command Handling Fail exit	0xA59F
// C2P mailbox Handling	
PSP C2P mailbox entry base [0xA5BX Cmd]	0xA5B0
Before send C2P command MboxBiosCmdDramInfo	0xA5B1
Before send C2P command MboxBiosCmdSmmInfo	0xA5B2
Before send C2P command MboxBiosCmdSleep SxInfo	0xA5B3
Before send C2P command MboxBiosCmdRsmlInfo	0xA5B4
Before send C2P command MboxBiosCmdQueryCap	0xA5B5
Before send C2P command MboxBiosCmdBootDone	0xA5B6
Before send C2P command MboxBiosCmdClearS3Sts	0xA5B7
Before send C2P command MboxBiosCmdS3DataInfo	0xA5B8
Before send C2P command MboxBiosCmdNop	0xA5B9
Before send C2P command MboxBiosCmdHSTIQuery	0xA5C4
Before send C2P command MboxBiosCmdClrSmmLock	0xA5C7
Before send C2P command MboxBiosCmdPciInfo	0xA5C8
Before send C2P command MboxBiosCmdGetVersion	0xA5C9
PSP C2P mailbox exit base [0xA5DX Cmd]	0xA5D0
Wait C2P command MboxBiosCmdDramInfo finished	0xA5D1
Wait C2P command MboxBiosCmdSmmInfo finished	0xA5D2
Wait C2P command MboxBiosCmdSleep SxInfo finished	0xA5D3
Wait C2P command MboxBiosCmdRsmlInfo finished	0xA5D4
Wait C2P command MboxBiosCmdQueryCap finished	0xA5D5
Wait C2P command MboxBiosCmdBootDone finished	0xA5D6
Wait C2P command MboxBiosCmdClearS3Sts finished	0xA5D7
Wait C2P command MboxBiosCmdS3DataInfo finished	0xA5D8
Wait C2P command MboxBiosCmdNop finished	0xA5D9
Wait C2P command MboxBiosCmdHSTIQuery finished	0xA5E4
Wait C2P command MboxBiosCmdClrSmmLock finished	0xA5C7
Wait C2P command MboxBiosCmdPciInfo finished	0xA5C8
Wait C2P command MboxBiosCmdGetVersion finished	0xA5C9
// fTPM command Handling [0xA5FX]	
PspfTpm send TPM command entry	0xA5F0
PspfTpm send TPM command exit	0xA5F1
PspfTpm receive TPM command entry	0xA5F2
PspfTpm receive TPM command exit	0xA5F3

5-11-6 [0xA9XX, 0xAAXX] assigned for AGESA NBIO Module

// NbioBase	
AmdNbioBase PEIM driver entry	0xA900
AmdNbioBase PEIM driver exit	0xA901
AmdNbioBase DXE driver entry	0xA902
AmdNbioBase DXE driver exit	0xA903
// PCIe	
AmdNbioPcie PEIM driver entry	0xA904
AmdNbioPcie PEIM driver exit	0xA905
AmdNbioPcie DXE driver entry	0xA906
AmdNbioPcie DXE driver exit	0xA907
// GFX	
AmdNbioGfx PEIM driver entry	0xA908
AmdNbioGfx PEIM driver exit	0xA909
AmdNbioGfx DXE driver entry	0xA90A
AmdNbioGfx DXE driver exit	0xA90B
// IOMMU	
AmdNbiolommu DXE driver entry	0xA90C
AmdNbiolommu DXE driver exit	0xA90D
// ALIB	
AmdNbioALIB DXE driver entry	0xA90E
AmdNbioALIB DXE driver exit	0xA90F
// SMU	
AmdSmuV8 PEIM driver entry	0xA910
AmdSmuV8 PEIM driver exit	0xA911
AmdSmuV8 DXE driver entry	0xA912
AmdSmuV8 DXE driver exit	0xA913
AmdSmuV9 PEIM driver entry	0xA914
AmdSmuV9 PEIM driver exit	0xA915
AmdSmuV9 DXE driver entry	0xA916
AmdSmuV9 DXE driver exit	0xA917
AmdSmuV10 PEIM driver entry	0xA918
AmdSmuV10 PEIM driver exit	0xA919
AmdSmuV10 DXE driver entry	0xA91A
AmdSmuV10 DXE driver exit	0xA91B
// IOMMU PEIM	
AmdNbiolommu PEIM driver entry	0xA920
AmdNbiolommu PEIM driver exit	0xA921
// APB DXE	
APCB DXE Entry	0xA922
APCB DXE Exit	0xA923

// APCB SMM	
APCB SMM Entry	0xA924
APCB SMM Exit	0xA925
// [0xA950, 0xA99F] NBIO PPI/PROTOCOL Callback	
NbioTopologyConfigureCallback entry	0xA950
NbioTopologyConfigureCallback exit	0xA951
MemoryConfigDoneCallbackPpi entry	0xA952
MemoryConfigDoneCallbackPpi exit	0xA953
DxioInitializationCallbackPpi entry	0xA954
DxioInitializationCallbackPpi exit	0xA955
DispatchSmuV9Callback entry	0xA956
DispatchSmuV9Callback exit	0xA957
DispatchSmuV10Callback entry	0xA958
DispatchSmuV10Callback exit	0xA959
AmdPcieMisclnit Event entry	0xA95A
AmdPcieMisclnit Event exit	0xA95B
NbioBaseHookReadyToBoot Event entry	0xA95C
NbioBaseHookReadyToBoot Event exit	0xA95D
NbioBaseHookPciO Event entry	0xA95E
NbioBaseHookPciO Event exit	0xA95F
// [0xA980, 0xA99F] BR GNB Task	
GnbEarlyInterfaceCZ entry	0xA970
GnbEarlyInterfaceCZ exit	0xA971
PcieConfigurationInit entry	0xA972
PcieConfigurationInit exit	0xA973
GnbEarlierInterfaceCZ entry	0xA974
GnbEarlierInterfaceCZ exit	0xA975
PcieEarlyInterfaceCZ entry	0xA976
PcieEarlyInterfaceCZ exit	0xA977
PciePostEarlyInterfaceCZ entry	0xA978
PciePostEarlyInterfaceCZ exit	0xA979
GfxConfigPostInterfaceCZ entry	0xA97A
GfxConfigPostInterfaceCZ exit	0xA97B
GfxPostInterfaceCZ entry	0xA97C
GfxPostInterfaceCZ exit	0xA97D
GnbPostInterfaceCZ entry	0xA97E
GnbPostInterfaceCZ exit	0xA97F
PciePostInterfaceCZ entry	0xA980
PciePostInterfaceCZ exit	0xA981
GnbEnvInterfaceCZ entry	0xA982
GnbEnvInterfaceCZ exit	0xA983

GfxConfigEnvInterface entry	0xA984
GfxConfigEnvInterface exit	0xA985
GfxEnvInterfaceCZ entry	0xA986
GfxEnvInterfaceCZ exit	0xA987
GfxMidInterfaceCZ entry	0xA988
GfxMidInterfaceCZ exit	0xA989
GfxIntInfoTableInterfaceCZ entry	0xA98A
GfxIntInfoTableInterfaceCZ exit	0xA98B
PcieMidInterfaceCZ entry	0xA98C
PcieMidInterfaceCZ exit	0xA98D
GnbMidInterfaceCZ entry	0xA98E
GnbMidInterfaceCZ exit	0xA98F
GnbSmuMidInterfaceCZ entry	0xA990
GnbSmuMidInterfaceCZ exit	0xA991
InvokeAmdInitLate entry	0xA992
InvokeAmdInitLate exit	0xA993
GnbSmuServiceRequestV8 entry	0xA994
GnbSmuServiceRequestV8 exit	0xA995

5-11-7 [0xACXX] assigned for AGESA CCX Module

CCX IDS IDS_HOOK_CCX_AFTER_AP_LAUNCH	0xAC10
CCX PEI entry	0xAC50
CCX downcore entry	0xAC51
CCX DXE entry	0xAC55
CCX MP service callback entry	0xAC56
CCX Read To Boot callback entry	0xAC57
CCX SMM entry	0xAC5D
CCX PEI start to launch APs for S3	0xAC70
CCX PEI end of launching APs for S3	0xAC71
CCX start to launch AP	0xAC90
CCX launch AP is ended	0xAC91
CCX launch AP abort	0xAC92
CCX MP service abort	0xAC93
CCX cac weights	0xAC94
CCX PEI exit	0xACE0
CCX downcore exit	0xACE1
CCX DXE exit	0xACE5
CCX MP service callback exit	0xACE6
CCX Read To Boot callback exit	0xACE7
CCX SMM exit	0xACED

5-11-8 [0xADXX] assigned for AGESA DF Module

DF PEI entry	0xAD50
DF DXE entry	0xAD55
DF Ready to Boot entry	0xAD56
DF PEI exit	0xADE0
DF DXE exit	0xADE5
DF Ready to Boot exit	0xADE6

5-11-9 [0xAFXX] assigned for AGESA FCH Module

FCH InitReset dispatch point	0xAF01
FCH InitEnv dispatch point	0xAF06
FCH InitMid dispatch point	0xAF07
FCH InitLate dispatch point	0xAF08
FCH Inits3Early dispatch point	0xAF0B
FCH Inits3Late dispatch point	0xAF0C
FCH Inits3Early dispatch finished	0xAF0D
FCH Inits3Late dispatch finished	0xAF0E
FCH Pei Entry	0xAF10
FCH Pei Exit	0xAF11
FCH MultiFch Pei Entry	0xAF12
FCH MultiFch Pei Exit	0xAF13
FCH Dxe Entry	0xAF14
FCH Dxe Exit	0xAF15
FCH MultiFch Dxe Entry	0xAF16
FCH MultiFch Dxe Exit	0xAF17
FCH Smm Entry	0xAF18
FCH Smm Exit	0xAF19
FCH Smm Dispatcher Entry	0xAF20
FCH Smm Dispatcher Exit	0xAF21
FCH InitReset HwAcpi	0xAF40
FCH InitReset AB Link	0xAF41
FCH InitReset LPC	0xAF42
FCH InitReset SPI	0xAF43
FCH InitReset eSPI	0xAF44
FCH InitReset SD	0xAF45
FCH InitReset eMMC	0xAF46
FCH InitReset SATA	0xAF47
FCH InitReset USB	0xAF48
FCH InitReset xGbE	0xAF49
FCH InitReset HwAcpiP	0xAF4F
FCH InitEnv HwAcpi	0xAF50

FCH InitEnv AB Link	0xAF51
FCH InitEnv LPC	0xAF52
FCH InitEnv SPI	0xAF53
FCH InitEnv eSPI	0xAF54
FCH InitEnv SD	0xAF55
FCH InitEnv eMMC	0xAF56
FCH InitEnv SATA	0xAF57
FCH InitEnv USB	0xAF58
FCH InitEnv xGbE	0xAF59
FCH InitEnv HwAcpiP	0xAF5F
FCH InitMid HwAcpi	0xAF60
FCH InitMid AB Link	0xAF61
FCH InitMid LPC	0xAF62
FCH InitMid SPI	0xAF63
FCH InitMid eSPI	0xAF64
FCH InitMid SD	0xAF65
FCH InitMid eMMC	0xAF66
FCH InitMid SATA	0xAF67
FCH InitMid USB	0xAF68
FCH InitMid xGbE	0xAF69
FCH InitLate HwAcpi	0xAF70
FCH InitLate AB Link	0xAF71
FCH InitLate LPC	0xAF72
FCH InitLate SPI	0xAF73
FCH InitLate eSPI	0xAF74
FCH InitLate SD	0xAF75
FCH InitLate eMMC	0xAF76
FCH InitLate SATA	0xAF77
FCH InitLate USB	0xAF78
FCH InitLate xGbE	0xAF79
End of TP range for FCH	0xAFFF
Last defined AGESA PCs	0xFFFF

5-12 BIOS POST Beep code (AMI standard)

5-12-1 PEI Beep Codes

# of Beeps	Description
1	Memory not Installed.
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXE IPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

5-12-2 DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met